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Development of Micro-Hall Devices for Current Sensing

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Abstract

In this work, micro-Hall devices were developed for the purpose of sensing current within a high temperature and high power environment. GaAs HEMT, InGaAs pHEMT, and GaN HEMT structures were studied. These structures were grown by molecular beam epitaxy. Processing techniques including photolithography, metallization, Si deposition, wet etching, and dry etching were studied. Electrical characterization measurements including low frequency noise, Hall effect, sensitivity, capacitance-voltage, and current-voltage were performed.

Electron mobility and sheet carrier density studies were performed for both the InGaAs pHEMT and GaAs HEMT structures. Results indicated the InGaAs pHEMT was superior and thus fabricated as the micro-Hall device. The Hall mobilities for the InGaAs QW micro-Hall device were found to be 67,300 cm^2/Vs and 7,980 cm^2/Vs at 80 K and 290 K respectively. The sheet density was found to be 5.3×10^{11} cm^{-2} and 4.2×10^{11} cm^{-2} at 80 K and 290 K, respectively. Deep level noise spectroscopy was performed and two active electron traps that degrade the magnetic field detection limit were discovered. The minimum detectable magnetic field of 2.5×10^{-9} T at 80 K and 100 kHz was recorded. A mobility decrease and an increase in carrier density were found at temperatures above 500 K, further contributing to the degradation in device performance. The Hall mobility and sheet density recorded for this device at 550 K was 1160 cm^2/Vs and 4.2×10^{12} cm^{-2}.

Due to the wide band gap and high peak electron drift velocity, GaN/AlGaN HEMT structures were studied as an alternative material system to the GaAs/InGaAs/AlGaAs QW structures. The GaN/AlGaN material system was optimized with respect to high electron mobility and low electron density. It was found that buffer layer thickness, AlGaN barrier thickness, and Al composition in the AlGaN layer had dramatic effects on mobility and electron

sheet carrier density. Based on these findings, the GaN/$Al_{0.21}Ga_{0.79}N$/GaN structure was found most appropriate for the fabrication of the micro-Hall effect device. For this structure, Hall mobilities of 15,300 cm^2/Vs and 1,400 cm^2/Vs and sheet electron densities as high as 6×10^{12} cm^{-2} and 1.0×10^{13} cm^{-2} were measured at 8 K and 295 K, respectively.

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Chapter 1: Introduction and Research Methodology

1.1 Introduction

Current sensing in circuits is important for reasons such as circuit protection and safety. On a small scale, current sensing can serve as a gauge for battery life. On a larger scale, current sensing can monitor how efficient a motor is performing. In almost any case, knowing how much current a circuit is carrying is a variable tool to protect more expensive equipment from a current overload situation [1].

There are many different types of current sensors on the market, several of which are discussed in the following section. Of these different types, the Hall sensor was the focus of this thesis for reasons that are detailed below. Two semiconducting materials, GaAs and GaN, make up the majority of the devices. Due to the fact that GaAs growth is a mature process, a large portion of this work involved the development of GaN growth techniques and understanding GaN/AlGaN heterojunctions.

In this chapter reviews of current sensing technology and the Hall effect are given in Sections 1.2 and 1.3 respectively. An overview of characterization techniques is discussed in Section 1.4. Development of GaAs-based and GaN-based micro-Hall devices are explained in Chapters 2 and 3 respectively. Conclusions and future work is detailed in Chapter 4.

1.2 Current Sensing Technology

Current sensors are classified as either direct or indirect. A direct sensor must be physically attached to the circuit at the point of interest. An indirect sensor does not have to be attached to the circuit at the point of interest, but will need a separate power source. Depending on the

application, the power to operate an indirect sensor may be much less than the power wasted by using a direct sensor [1]. Below is a review of direct and indirect current sensing technologies.

1.2.1 Direct Current Sensors

Direct current sensors make use of Ohm's law, which is why they are connected to the circuit at the point where the current is being monitored. For this reason, direct current sensors are simply resistors and are given the name shunt resistors. Because shunt resistors are connected to the circuit at the point of interest, they are very fast and very sensitive. The main drawback to these sensors is that all resistors dissipate power based on the following equation [2]

$$P = I^2R. \tag{1}$$

It is easy to see from Eq. 1 that as the current through the resistor is increased, the power dissipated increases very rapidly. Power dissipated as heat is not only inefficient but can also degrade circuit board performance [1].

1.2.2 Indirect Current Sensors

The purpose of indirect current sensors is to achieve electrical isolation. In cases involving a high current load, electrical isolation can increase the efficiency of the circuit by decreasing the power dissipated. The main different types of indirect current sensors are [1]

1. Rogowski Coil
2. Current Transformer
3. Fluxgate Sensor
4. Hall Effect Sensor

The Rogowski coil is a type of indirect current sensor that can detect high frequency currents. The coil is made up of a wire that is wrapped in a helical shape. When the wrapping forms a toroid, the lead end is passed back through the helix and is returned to the starting point. The coil is therefore open, creating an easily installable sensor. Rogowski coils must be wrapped around the wire of interest and thus cannot be used in integrated circuits.

The current transformer, like the Rogowski coi,l is usually a toroid wrapped around the wire of interest. A transformer contains a primary winding and a secondary winding. Current through the primary winding induces a current through the secondary winding. The induced current is alternating, which may not be favorable in many circumstances [1].

The fluxgate sensor is much like the current transformer. There are two windings involved, a drive winding and a sense winding. The drive winding is usually wrapped around a toroid. The sense winding is folded around the entire toroid (center included). The output signal of the sense coil is changed when fluxgate sensor is in the presence of an external magnetic field. The change in the current of the sense winding is proportional to the magnetic field. Fluxgate sensors, like the other indirect sensors, are too large for integrated circuits [1].

The Hall effect sensor is a magnetic field sensor made out of semiconducting material. Hall sensors can sense both DC and AC signals. Hall sensors can be made very small (micrometer) in order to fit easily in integrated circuits [1], and, at the same time, they can sense magnetic fields in the nT range.

Another aspect of the Hall effect sensor that sets it apart from other indirect current sensors is the fact that as long as a magnetic field is present, the sensor can measure current. This means that a Hall effect sensor can make DC measurements. One example of this type of circuit is given in Fig. 1, which shows an inverter with an H-bridge configuration. An H-bridge is found in

hybrid and electric cars that contain AC motors where a large amount of current flows through each switching position. If the amount of current is high enough, multiple transistors will be needed in parallel within each switching position. If the resistance of one transistor increases over time, the other transistors in parallel will begin to take on more current possibly resulting in burn out. A current sensor is needed in order to communicate with the gate drivers by sending a signal to increase or decrease gate voltages in order to level the current load [1]. Components such as inverters need to be as efficient as possible in environments such as hybrid and electric vehicles. Hall effect sensors provide an increase in inverter efficiency because they measure current indirectly. The Hall sensor is explained in detail in Section 1.4.

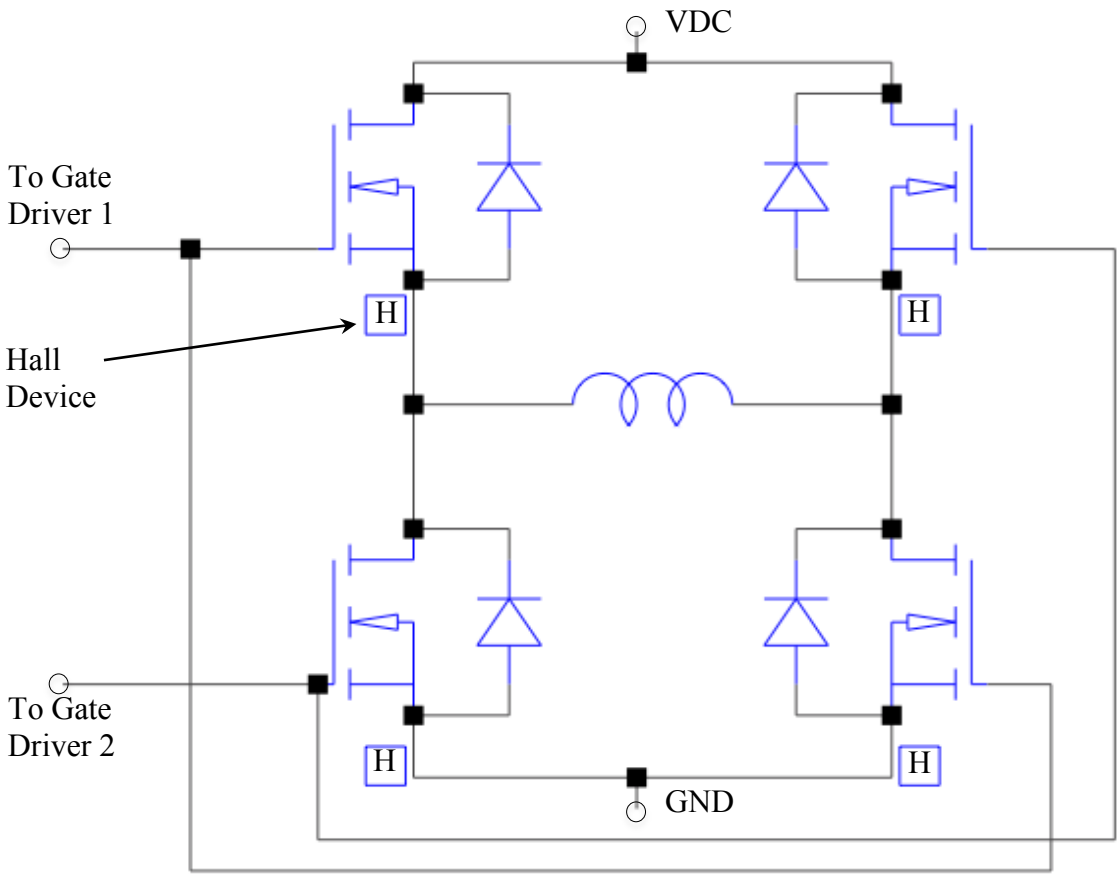

Fig. 1. H-Bridge with Hall devices sensing current that passes though the transistors.

1.3 Research Method

The research methodology was as follows. GaAs quantum well (QW) and InGaAs QW material systems with a known high mobility were processed as a micro-Hall device. The GaAs-based devices were provided and only required minimal processing in order to be characterized. For this reason, the description of MBE and processing details are explained with respect to GaN. The GaAs-based devices were characterized by methods described in Section 1.4.

Due to a project requirement of high temperature device operation, GaN structures were chosen in order to increase stability over a wide temperature range due to the material's wide band gap. Overall, twelve GaN-based structures were grown varying layer thicknesses, alloy compositions, and substrates in order to achieve the highest mobility and optimal carrier concentration. The details of these growths are given in Section 3.6. The grown samples were then processed (Section 3.7) and initial characterization techniques have been performed. The results are given in Section 3.8. The conclusion and proposed future research is given in Chapter 4.

The sample naming convention used throughout this thesis was the same naming convention used in the Molecular Beam Epitaxy Lab at the University of Arkansas. There was no meaning to the naming convention as the use was simply a method to catalog growth details and recipes. See Apendix H for cross sectional diagrams and growth recipes for each GaN-based structure described in this thesis.

1.4 Review of the Hall Effect

The Hall effect was discovered in 1879 by Edwin H. Hall. His research involved the study of the magnetic field effects on current in a wire. Hall was working with gold foil when he

discovered a voltage appearing across a sample perpendicular to the voltage that was applied. The voltage appeared when the sample was in the presence of a magnetic field perpendicular to the sample surface. The underlying physics behind the induced voltage Hall discovered is still used for characterizing semiconductors today and can be exploited to develop magnetic field sensors [3]. The physics of the Hall effect beginning with the Lorentz force is explained in this section.

The equation describing the Lorentz force is [3]

$$\boldsymbol{F}_L = q(\boldsymbol{v}_d \times \boldsymbol{B}) \tag{2}$$

where $\boldsymbol{F}_L$ is the Lorentz force, q is the fundamental charge, $\boldsymbol{v}_d$ is the charge carrier drift velocity and $\boldsymbol{B}$ is the applied magnetic field. The Lorentz force will be perpendicular to the drift velocity and magnetic field [4].

A pictorial representation of the Hall effect using an n-type bar is shown in Fig. 2. The n-type bar is a bulk semiconducting material in the shape of a rectangular box with electrons as the majority carrier. A voltage is then applied to the bar. When charge carriers are in the presence of an electric field ($\boldsymbol{E}_e$), the Coulombs force ($\boldsymbol{F}_C$) [4]

$$\boldsymbol{F}_C = q\boldsymbol{E}_e \tag{3}$$

acts on the charge. This force pushes the electron, giving rise to a velocity that is in the direction shown in Fig. 2.

In order to sense current, the Hall bar needs to create an output voltage that is proportional to current through a wire. A current carrying wire produces a magnetic field proportional to the bias current in the direction about the wire as in accordance with the right hand rule. This magnetic field is given by the Biot-Savart law, which is [4]

$$\boldsymbol{B} = \frac{\mu_0}{4\pi} \int \frac{Id\vec{l} \times \vec{r}}{|\vec{r}|^3} \tag{4}$$

where μ_0 is the permeability of free space and r is the distance from the wire to the point of measurement.

In the above example, the electron has a charge, velocity and an applied electric field. If the bar is placed near a current carrying wire, the external magnetic field induces a force that is perpendicular to both the velocity and the magnetic field as described by Eq. 4. This force will push electrons to one side of the bar while the other side of the bar will have a lack of electrons. This will result in an electric field ($\boldsymbol{E}_H$), called the Hall field. Thus, there will appear a force, which acts on the electron that is equal in magnitude and opposite in direction of the Lorentz force allowing charges to continue moving from the negative terminal to the positive terminal. $\boldsymbol{E}_H$ can be measured experimentally as the Hall voltage (V_H) [3].

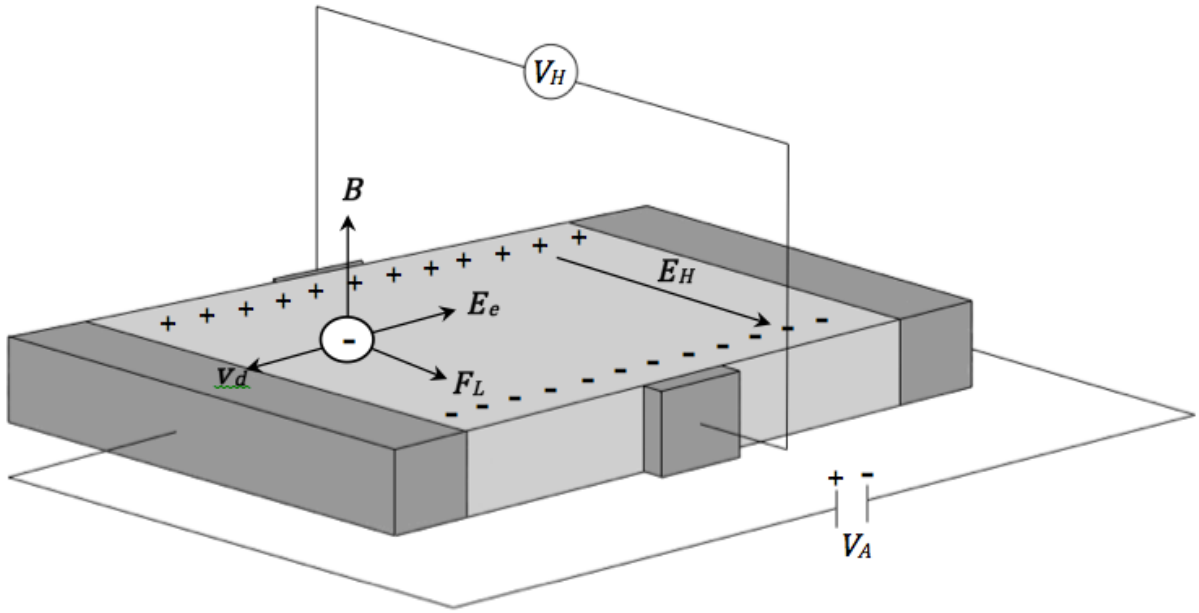

Fig. 2. n-type Hall bar with an applied voltage of V_A and external magnetic field of B. E_e is the electric field from the applied voltage. v_d is the electron drift velocity. F_L is the Lorentz force. E_H is the Hall electric field and V_H is the corresponding Hall voltage.

The derivation of V_H begins with equating the Lorentz force with the Coulomb force [4]

$$\boldsymbol{F}_H = q\boldsymbol{E}_H, \tag{5}$$

which results in [4]

$$\boldsymbol{E}_H = -(\boldsymbol{v}_d \times \boldsymbol{B}). \tag{6}$$

Integrating $\boldsymbol{E}_H$ across the width of the Hall bar gives [3]

$$V_H = \int \boldsymbol{E}_H \, d\boldsymbol{r} \tag{7}$$

or [3]

$$V_H = v_d BWG \tag{8}$$

where W is the width of the Hall bar and G is a geometrical correction factor.

The key aspect of the Hall effect is the Lorentz force that acts on charges creating the Hall electric field. The main components to the Lorentz force are the drift velocity and the external magnetic field. As far as device design is concerned, there is no control over how strong an external magnetic field is. Therefore, the drift velocity must be maximized in order to maximize the Lorentz force. Thus, the ability of the device to detect smaller magnetic fields depends on the speed of the electrons. The faster the electrons the more responsive to a change in magnetic field (sensed current) the device will be [3].

The relationship between drift velocity and electric field for electrons is given by [5]

$$v_d = \mu E_e \tag{9}$$

where μ is the electron mobility. The magnitude of the applied electric field can be written as [5]

$$E_e = \frac{V_A}{L} \tag{10}$$

where V_A is the applied voltage and L is the length of the device. Substituting Eqs. 9 and 10 into Eq. 6 gives [3]

$$\boldsymbol{E}_H = (\frac{\mu V_A}{L} \vec{e} \times \boldsymbol{B}) \tag{11}$$

where $\vec{e}$ is the unit vector in the direction of v_d. Substituting Eq. 11 into the voltage/electric relationship and taking the integral over the width of the device results in the Hall voltage equation as a function of applied voltage which is [3]

$$V_H = \frac{\mu W}{L} V_A B G. \tag{12}$$

V_H as a function of applied current can also be derived. Using Ohm's Law, $V = IR$, and a resistance of $R = L/(\sigma w t)$ [5], Eq. 12 can be written as [3]

$$V_H = \frac{\mu G}{\sigma t} I B \tag{13}$$

where I is the bias current. Substituting the equation for conductivity ($\sigma = qn\mu$) into Eq. 13 results in [3]

$$V_H = \frac{G}{q n_{2D} t} I B \tag{14}$$

where n_{2D} is the electron density.

One can see from Eqs. 12 and 14 that in order to increase the Hall voltage output, mobility must be high and carrier density must be low. Furthermore, if the sensitivity of the device is defined as the rate of change of Hall voltage with respect to the rate of change of the magnetic field, then increasing μ and decreasing n_{2D} will result in a more sensitive Hall effect sensor [3].

Sensitivity of a Hall effect sensor is one of the most important characteristics to be concerned with, especially when considering an environment with temperatures ranging from 150 °C to 300 °C. When the temperature increases, atoms within a solid begin to vibrate causing electrons to scatter on lattice phonons, which decreases mobility. Also, increasing temperatures cause electrons to gain energy and leave donors, which allows more electrons to take part in conduction, increasing n_{2D} leading to a degradation in device performance [3].

1.5 Methods of Characterization

Characterization of the micro-Hall device structures was performed through Hall effect measurements, low-frequency noise measurements, and sensitivity measurements [3]. These experimental methods helped to determine the quality of the growth and the potential range of device performance. Each method is explained in detail in this section.

1.5.1 Hall Effect Measurements

The Van der Pauw method was used for all Hall effect measurements performed and will be briefly explained here. Using this method requires that samples be processed in such a way as to meet the following conditions [3] [6]:

1. the contacts are located at edges of the sample;
2. the contacts are ohmic and sufficiently small;
3. the sample is of uniform thickness; and
4. the sample does not contain physical holes (area with no material).

Fig. 3 depicts a square sample with contacts that are much smaller than the surface area of the sample. If Contacts 1 and 2 are biased in such a way that current flows into Contact 1 and out of Contact 2 (I_{12}), then a voltage will appear across Contacts 3 and 4. The voltage drop V_{34} is defined as $V_3 - V_4$. A resistance can be defined such that [6] [7]

$$R_{12,34} = \frac{V_{34}}{I_{12}}. \tag{15}$$

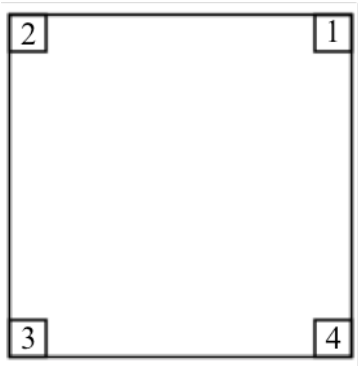

Fig. 3. Square sample with relatively small contacts labeled as 1,2,3, and 4.

Two measurements are required in order to determine a sheet resistance, therefore another resistance is defined such that [7]

$$R_{23,41} = \frac{V_{41}}{I_{23}}. \tag{16}$$

The following relationship has been shown to hold true [6],

$$\exp\left(-\pi \frac{R_{12,34}}{R_S}\right) + \exp\left(-\pi \frac{R_{23,41}}{R_S}\right) = 1. \tag{17}$$

Eq. 17 can be rewritten as [7]

$$R_s = \frac{\pi}{\ln(2)} \frac{R_{23,41}+R_{23,41}}{2} F \tag{18}$$

where F is a function of $R_{12,34}/R_{23,41}$ such that [7]

$$\frac{R_{12,34}/R_{23,41}-1}{R_{12,34}/R_{23,41}+1} = \frac{F}{\ln(2)} \cosh^{-1}\left(\frac{\exp[\ln(2)/F]}{2}\right). \tag{19}$$

If two contacts that are not side by side are biased, such as 2 and 4, then a Hall voltage will appear across 1 and 3 as explained in Section 1.3. The Hall voltage across Contacts 1 and 3 is given by Eq. 14 and can be solved for n. Once n is known the mobility can then be calculated [7].

1.5.2 Noise Measurements

Noise measurements are made in order to gain a deeper understanding of the device quality. The primary goal of noise measurements is to study defects within the device volume. Defects are caused by lattice imperfections as well as impurity atoms. Defects allow for deep states (electrically active traps) to appear within the band gap of the device, which serve as centers of generation and recombination (G-R) of carriers. These defects increase low frequency noise, which decrease device performance [8]. There are three types of low frequency noise that can be found within a Hall effect device, which are 1/f noise, G-R noise, and thermal noise [3].

While the origin of 1/f noise is disputed, phenominologically it has been shown to follow the following functional form [3],

$$S_{1/f} = I^2 \frac{\alpha}{N} \frac{1}{f} = V^2 \frac{\alpha}{N} \frac{1}{f} \tag{20}$$

where I and V are the bias current and applied voltage respectively, α is the Hooge parameter, N is the number of charge carriers in the device volume, and f is the frequency. The Hooge parameter is a dimensionless material parameter related to material quality and is found through experimental results [3]. $1/f$ noise is thought to originate from either fluctuation in mobility or carrier density. Therefore, the Hooge parameter is either an indication of the amount of scattering or G-R centers within the sample [9]

G-R noise is due to the independent random nature of generation and recombination phenomena. Because carrier generation and recombination occur independently about an equilibrium, the number of free carriers in the device volume will also fluctuate giving rise to noise. G-R noise will be dependent on the carrier lifetime and is modeled by [3]

$$S_{G-R} = \frac{BI^2 4\tau}{1+(2\pi f\tau)^2} \tag{21}$$

where B is a material parameter and τ is the carrier lifetime given by [8]

$$\frac{1}{\tau} = \frac{1}{\tau_{emission}} + \frac{1}{\tau_{capture}} . \quad (22)$$

Thermal noise is due to the random impeded movement of free carriers caused by lattice vibrations and is given by [3]

$$S_{Thermal} = 4kTR \quad (23)$$

where k is Boltzmann's constant, T is the temperature in Kelvin, and R is the device resistance.

In order to extract the material parameters that are unknown in the above equations, the total noise can be modeled by adding the three components together forming the fitting equation

$$S_{noise} = \frac{A}{f} + \sum_i \frac{C_i}{1+(f/f_{0i})^2} + 4kTR \quad (24)$$

where A is the amplitude of the 1/f noise, f is the signal frequency, $f_{0i} = 1/2\pi\tau_i$, C_i is the amplitude of the G-R noise due to the i^{th} g-r center and τ_i is the time constant [3].

Plots of the noise spectrum as a function of temperature can indicate the presence of the G-R centers. This is because the Fermi level within the device volume changes with respect to the trap levels as temperature changes.

G-R noise can also be written as [8]

$$S_{G-R} = A\frac{\tau F(1-F)}{1+(\omega\tau)^2} \quad (25)$$

where $A = 4N_t/VN_t^2$, $\tau = \tau_C F = F(\sigma v_T n_0)^{-1}$, and ω is the angular frequency. Here, V is the volume of the sample, σ is the cross sectional area of the trap, v_T is the electron thermal velocity, and n_0 is the equilibrium electron concentration. Using the conduction band edge as the reference and considering the valence band to be located at a positive energy (Fig. 4) then the occupancy of the trap at energy E_0 is given by [8]

$$F(E_0) = \frac{1}{1+\exp\left[\frac{E_F-E_0}{kT}\right]} . \quad (26)$$

Fermi energy (E_F) is given by

$$E_F = kTln\left(\frac{N_C}{N_D}\right) \tag{27}$$

where N_C is the density of states and N_D is the donor concentration.

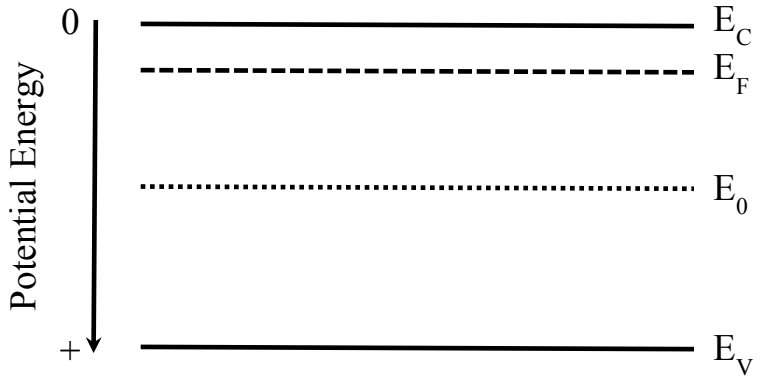

Fig. 4. Energy band diagram of an n-type semiconductor with a trap level E_0.

If the trap cross sectional area depends on temperature by $\sigma = \sigma_0 \exp(-E_1/kT)$, then the capture time constant can be written as $\tau = \tau_{C0}\exp(E_1/kT) = (\sigma v_T n_0)^{-1}\exp(E_1/kT)$. Now Eq. 25 can be written as [8]

$$S_{G-R} = A\frac{\tau_{C0}\exp\left(\frac{E_1}{kT}\right)F^2(1-F)}{1+\omega^2\tau_{C0}^2\exp\left(\frac{2E_1}{kT}\right)F^2}. \tag{28}$$

Considering the case of a high electron concentration, the Fermi level will be located close to the conduction band edge. Again, considering the conduction band as the reference, E_0 will likely be much greater than E_F as shown in Fig. 4. In this case, $F \approx 1$ and

$$1 - F = \exp\left(-\left(\frac{E_0 - E_F}{kT}\right)\right). \tag{29}$$

Substituting Eq. 27 into Eq. 29 yields

$$1 - F = \frac{N_C}{N_D}\exp\left(-\left(\frac{E_0}{kT}\right)\right). \tag{30}$$

Now Eq. 28 can be written as [8]

$$S_{G-R} = A\tau_{C0}\frac{N_C}{N_D}\frac{\exp\left(\frac{E_1-E_0}{kT}\right)}{1+\omega^2\tau_{C0}^2\exp\left(\frac{2E_1}{kT}\right)}. \tag{31}$$

Considering Eq. 31, solving $\frac{dS_{G-R}}{d(1/T)} = 0$ for $1/kT$ gives

$$\frac{1}{kT_{max}} = \frac{1}{2E_1} \ln \frac{E_1 - E_0}{(E_1 + E_0)\omega^2 \tau_{C0}^2} \tag{32}$$

or

$$\frac{1}{kT_{max}} = \frac{1}{2E_1} \ln \frac{E_1 - E_0}{(E_1 + E_0)\tau_{C0}^2} - \frac{1}{E_1} \ln \omega. \tag{33}$$

From Eq. 33, one can see that the slope of $1/kT_{max}$ versus ln ω is $-1/E_1$. Substituting Eq. 32 into Eq. 31 yields

$$S_{G-R,max} = A\tau_{C0} \frac{N_C}{N_D} \frac{\left(\frac{a}{\omega^2 \tau_{C0}^2}\right)^{\left(\frac{E_1 - E_0}{2E_1}\right)}}{1+a} \tag{34}$$

where

$$a = \frac{E_1 - E_0}{E_1 + E_0}. \tag{35}$$

Taking the natural log of $S_{G-R,max}$ gives

$$\ln S_{G-R,max} = \ln \frac{A\tau_{C0} N_C}{N_D(1+a)} \left(\frac{a}{\tau_{C0}^2}\right)^{\left(\frac{E_1 - E_0}{2E_1}\right)} - \frac{E_1 - E_0}{E_1} \ln \omega. \tag{36}$$

The slope of a ln $S_{G-R,max}$ versus ln ω is $-\frac{E_1 - E_0}{E_1}$. DLNS was used to discover traps within the InGaAs QW micro-Hall device. The data is shown in Section 2.3.3

The test setup for noise measurements is shown in Fig. 5. An adjustable (12/24 V) battery pack with tunable resistance was connected to the micro-Hall device mounted inside an MMR cryostat. The output voltage was passed through a SRS low noise pre-amplifier (Model SRS560). A SRS 2 channel dynamic signal analyzer (model SR785) was then used to perform FFT analysis. A MMR K-20 temperature controller was used to adjust the temperature within the cryostat.

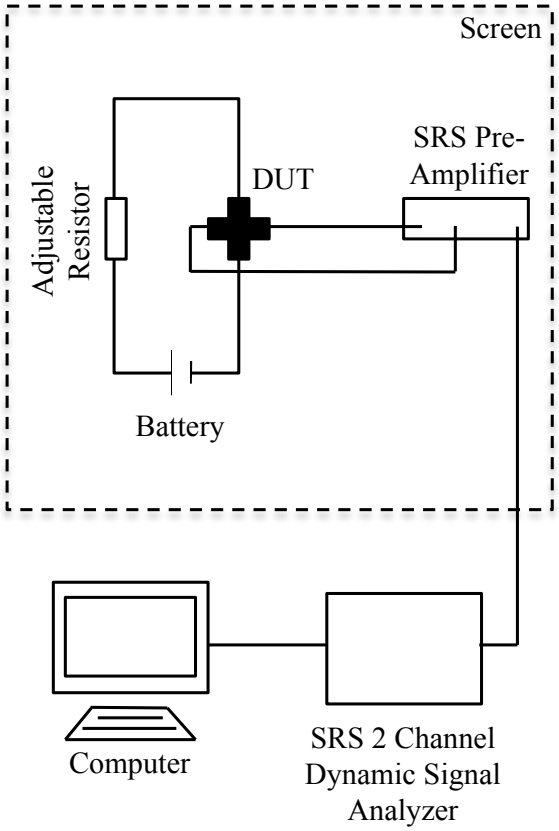

Fig. 5. Test setup for noise measurements.

1.5.3. Sensitivity Measurements

Sensitivity is a measure of the device's ability to detect magnetic fields. There are two types of sensitivity, absolute and normalized. Absolute sensitivity is defined as [3]

$$S_A = \frac{V_H}{B} \tag{37}$$

which is a ratio of the output voltage to the input magnetic field. The absolute sensitivity can be normalized by the biasing condition when divided by supplied voltage or current and yields

$$SVRS = \frac{S_A}{V} \tag{38}$$

or

$$SCRS = \frac{S_A}{I}. \quad (39)$$

$SVRS$ and $SCRS$ are the supply voltage related sensitivity and supply current related sensitivity, respectively, and can be used as a merit of device efficiency [3].

Sensitivity measurements were made using a MMR system that produced a magnetic field in the rage of -0.25 T to 0.25 T perpendicular to the device. A MMR K-20 temperature controller was used to vary the temperature (80 K to 550 K) of the stage within an MMR cryostat. The device was biased with a Keithley 236 source measure unit. The output Hall voltage was measured with a Keithley 182 voltmeter. This test setup is shown in Fig. 6.

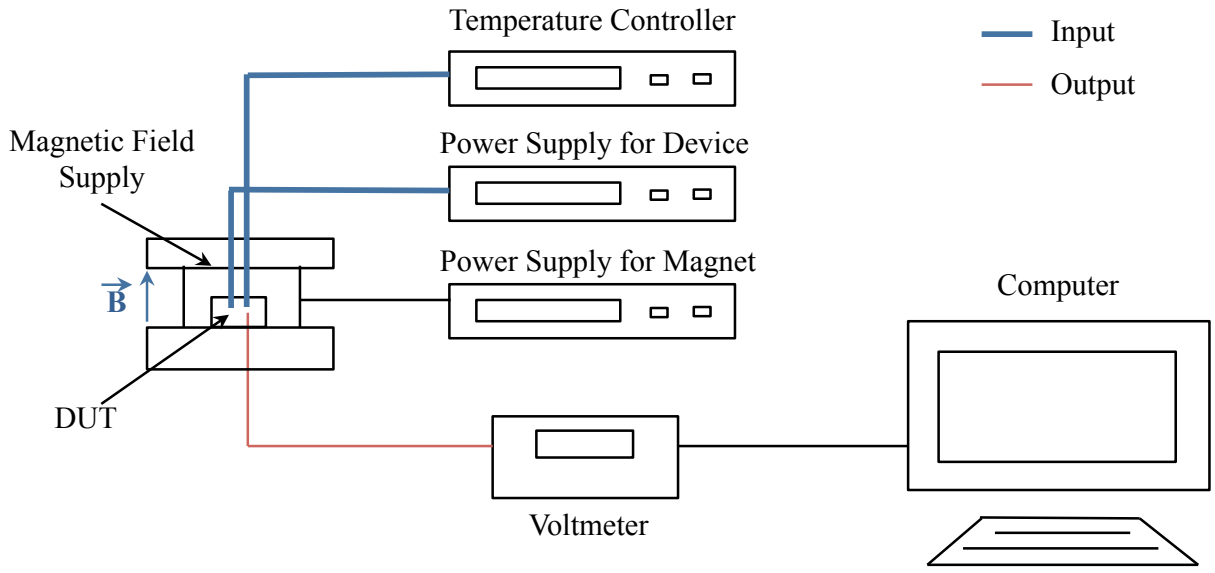

Fig. 6. Test setup for sensitivity measurements.

Chapter 2: Development of GaAs QW and InGaAs QW based Micro-Hall Devices

GaAs is a semiconducting material that has been studied heavily because of the materials wider band gap, high electron drift velocity, and high mobility when compared to silicon. GaAs is also a direct band gap material and therefore can be used to produce different electronic and optical devices, such as solar cells and laser diodes [10].

In this chapter, the physical and electrical properties of GaAs are discussed. A brief explanation of the growth and processing of GaAs and InGaAs quantum well micro-Hall devices is given followed by an in depth discussion of characterization results.

2.1 Physical and Electrical Properties of GaAs and InGaAs Structures

GaAs, AlGaAs, and InAs crystalize in a cubic zinc blende structure [15]. This structure is shown in Fig. 7 for GaAs with an *a* lattice parameters of 5.653 Å [16]. GaAs has a 1.43 eV band gap and an electron affinity of 4.07 eV at 300 K. These parameters are listed in Table 1 for GaAs, InGaAs, and AlGaAs [15]. The wide band gap of AlGaAs and the narrow band gap of InGaAs can be used to create a QW with relatively high barriers.

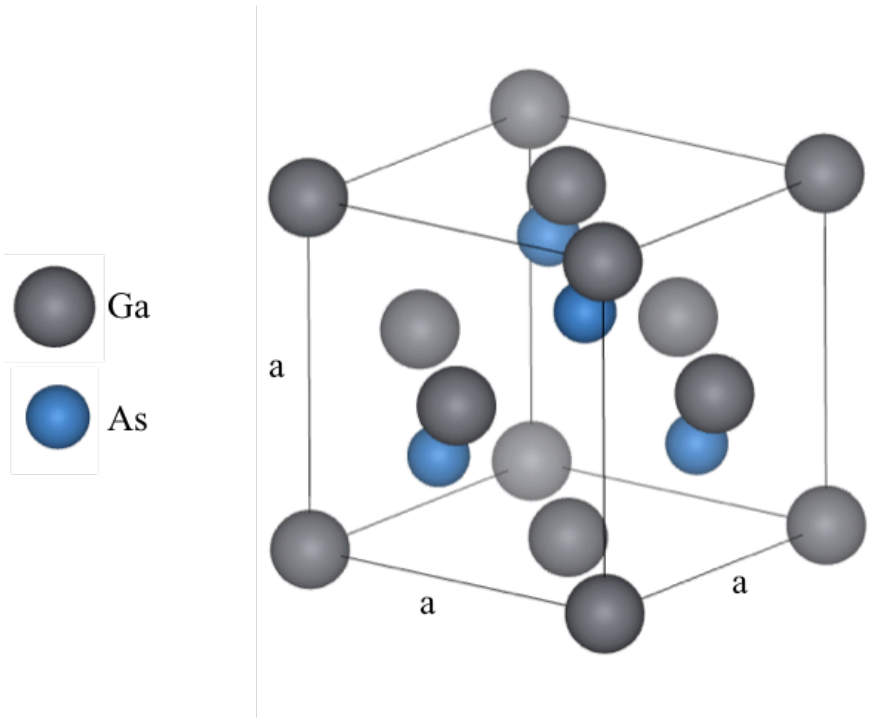

Fig. 7. Zinc blende cubic structure of GaAs.

Table 1. Physical and Electrical Properties of GaAs and InGaAs at 300 K [15]

Parameter	Units	GaAs	InAs	$Al_xGa_{1-x}As$
E_G	eV	1.43	0.354	1.424 + 1.247x
Lattice Constant *a*	Å	5.653	6.058	6.65 + 0.0078x
Electron Affinity	eV	4.07	4.9	4.07 - 1.1x

2.2 Growth of GaAs-Based HEMT Structures

Growth of GaAs QW high electron mobility transistor (HEMT) and InGaAs QW pseudomorphic HEMT (pHEMT) structures shown in Fig. 8 was performed using a RIBER 32P MBE system. The buffer layers in both structures consisted of 200 nm GaAs epi layer, an

$Al_{0.3}Ga_{0.7}As$ (1.5 nm)/GaAs (1.5 nm) supperlattice (20 repetitions), and a 300 nm GaAs layer. Each layer of the buffer was grown a 580 °C. The growth temperature for the $In_{0.12}Ga_{0.88}As$ QW was 540 °C. The lower growth temperature allowed for a high quality InGaAs layer and thus accomplished defect free InGaAs/AlGaAs interface. The Si doped AlGaAs and GaAs layers were grown at 610 °C, allowing for accurate doping densities to be obtained. An undoped layer of $Al_{0.3}Ga_{0.7}As$ was grown between the QW and doped $Al_{0.3}Ga_{0.7}As$ layers, separating the ionized donors from the 2DEG, thus increasing electron mobility [17].

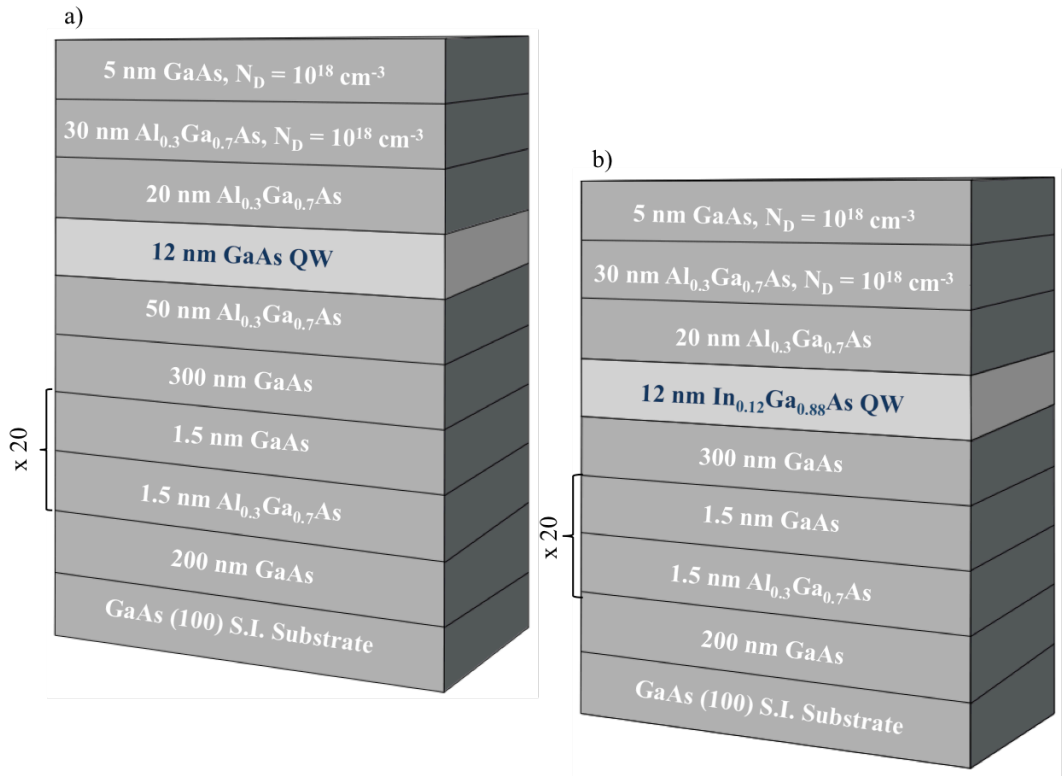

Fig. 8. Cross-sectional diagrams of (a) GaAs QW HEMT and (b) InGaAs QW pHEMT structures grown for characterization as micro-Hall devices.

The conduction band edge of the InGaAs QW structure (Fig. 8 (b)) is shown in Fig. 9 [18]. The QW was formed by the band offset of GaAs, InGaAs and AlGaAs (Table 1). The ionized

donors in the doped $Al_{0.3}Ga_{0.7}As$ layer created an electric field causing band bending and narrowing the conduction band edge and Fermi level separation [5]. The doped $Al_{0.3}Ga_{0.7}As$ layer was a possible location for parallel conduction.

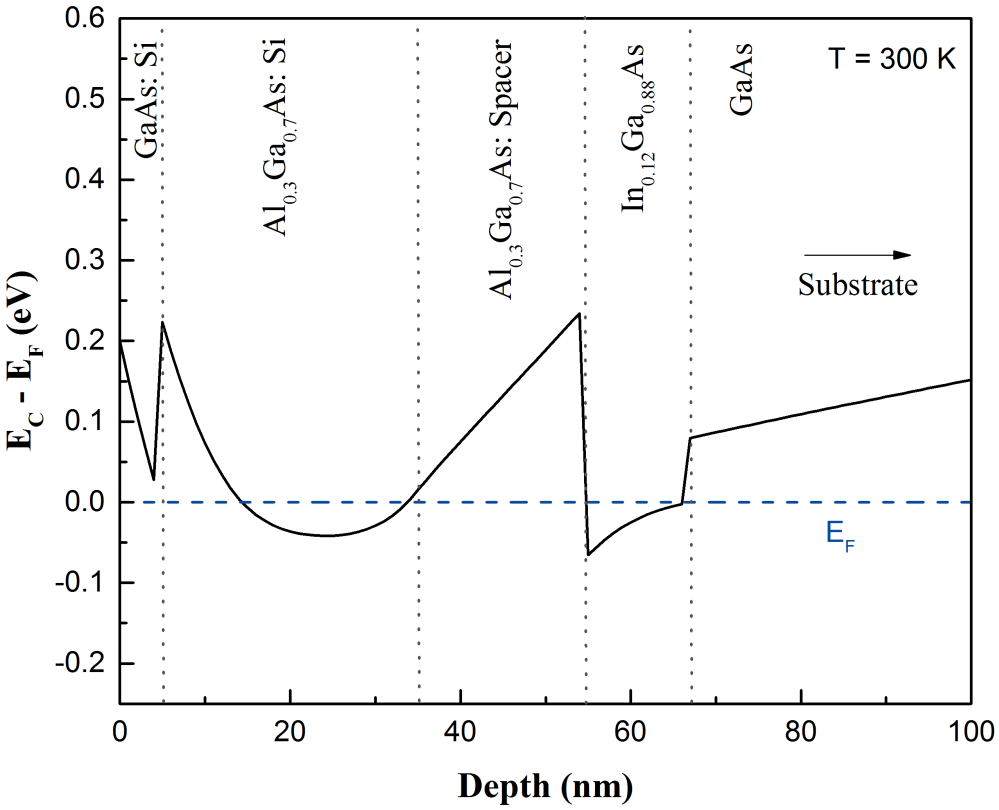

Fig. 9. Conduction band edge as a function of depth for InGaAs QW structure [17].

2.3 Characterization Results for GaAs QW and InGaAs QW Micro-Hall Devices

Hall measurements were made for GaAs QW and InGaAs QW micro-Hall devices. The mobility and sheet density for the InGaAs QW device were more stable over the temperature range of 80 K – 500 K than that of the GaAs QW device. Thus, the InGaAs QW device was further characterized by performing Hall effect measurements, low frequency noise

measurements, and sensitivity measurements. The results are discussed in depth within this section. Parameters, such as Hooge parameter and activation energies of traps were extracted.

2.3.1 Hall Measurements for GaAs QW and InGaAs QW Micro-Hall Devices

As stated earlier, Hall measurement data gives indication of device quality due to the dependence of performance on mobility and carrier concentrations [3]. Two different QW structures, GaAs QW (SE209) and InGaAs QW (SE210)) were processed as micro-Hall devices. Fig. 10 shows the Hall measurements over the temperature range of 80 K to 550 K for these devices. The mobility (Fig. 10 (a)) and carrier concentration (Fig. 10 (b)) of the two devices were approximately equivalent up to 500 K. At 500 K, the sheet density of the GaAs QW device increased at a much faster rate (95% difference). This increase in sheet density was reflected in the decrease in mobility. The InGaAs QW device was superior due to the lower rate of change of the mobility and sheet density at temperatures above 480 K. Evidence of parallel conduction in the doped AlGaAs layer that was mentioned in the previous section can be seen in Fig. 10 (a) by the increasing sheet density at temperatures below 150 K.

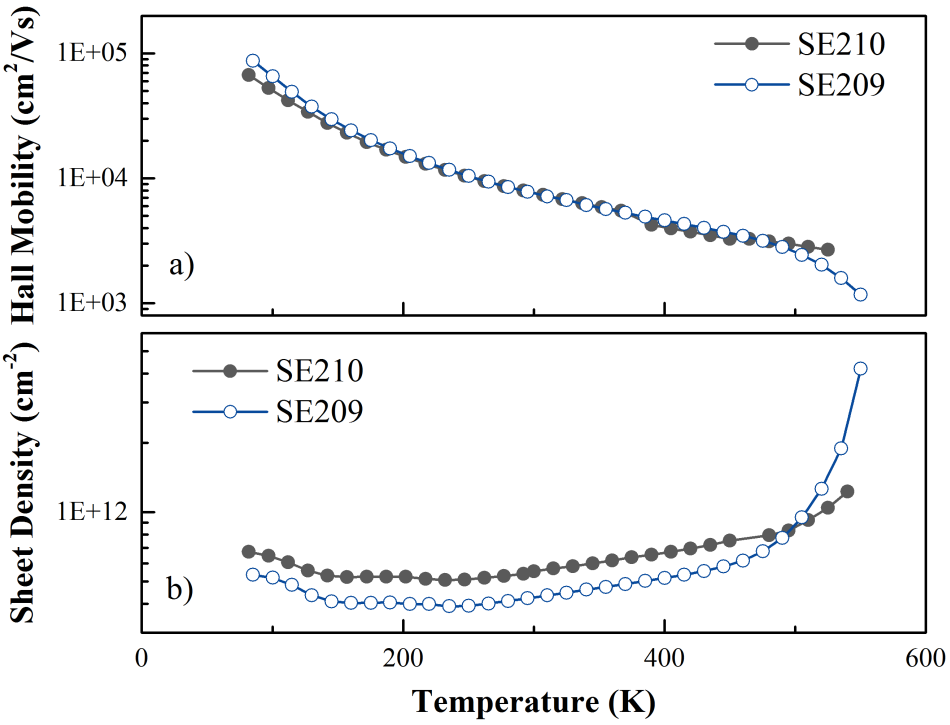

Fig. 10. Hall mobility and sheet density for SE209 and SE210.

2.3.2 Nonlinear Fit of Noise and Hooge parameter extraction

In order to extract unknown material parameters, the total noise of the InGaAs QW device, sample SE210, was modeled using Eq. 24 and is shown in Fig. 11. Also shown in Fig. 11 are the individual contributions of thermal, 1/*f*, and G-R noise. It was concluded from the two plateaus (bends in S_{GR-1} and S_{GR-2}) that two G-R centers were present within this sample.

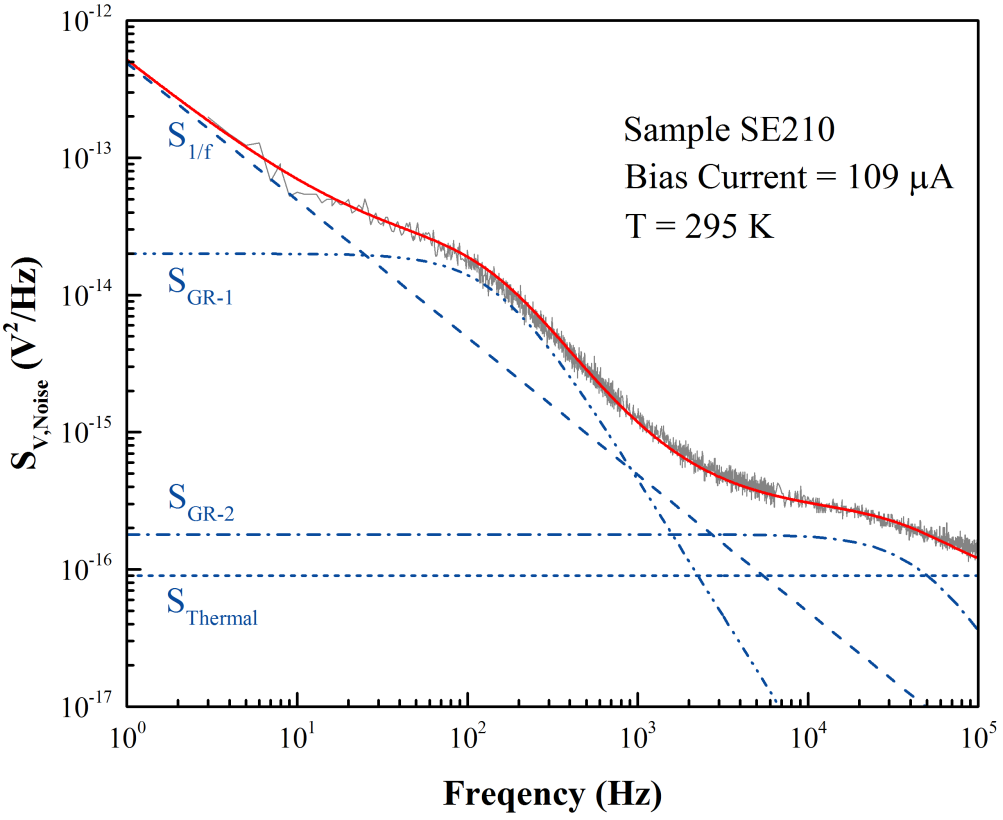

Fig. 11. Fitting of noise data for SE210 with a bias of 109 µA at room temperature.

The Hooge parameter is an indicator of crystalline quality and can be extracted from a noise versus frequency plot. Noting that the amplitude of 1/f noise can be written as $A = \alpha V^2/N$ (Eq. 20), the Hooge parameter can be described by [3]

$$\alpha = \frac{A}{V^2} \times N. \tag{40}$$

As shown above, the amplitude of the 1/f noise is directly proportional to α. The slope of the amplitude of $S_{V,1/f}$ vs. V^2 plot is then used to determine α. The noise data are shown in Fig. 12 and the amplitude of the 1/f noise is shown in Fig. 13.

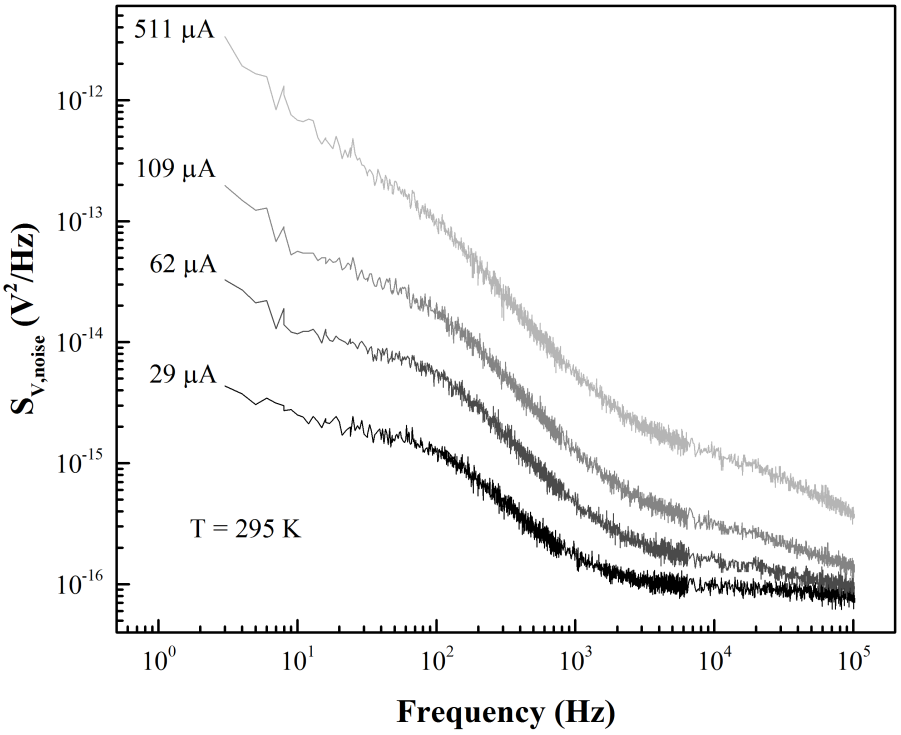

Fig. 12. Noise as a function of frequency for various bias currents for sample SE210.

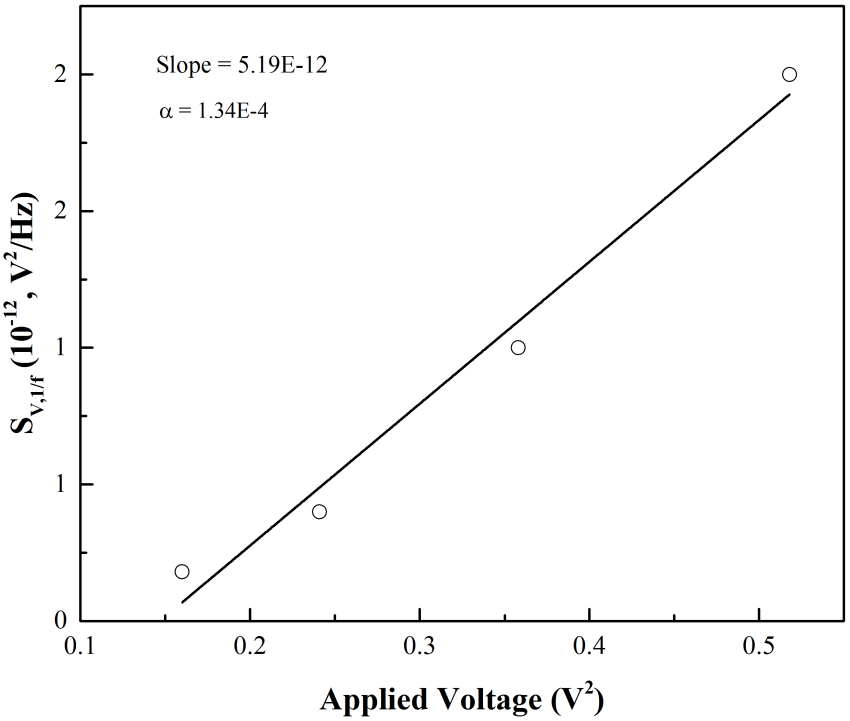

Fig. 13. Amplitude of 1/f noise used to find the Hooge parameter.

The equation describing the total number of carriers is [5]

$$N = \frac{L^2}{q\mu R} \tag{41}$$

where L is the length between contacts, q is the electron charge, μ is the mobility and R is the resistance of the sample. The Hall mobility was used for these calculations.

Again, the two major theories describing the origin of 1/*f* noise are fluctuations in mobility or carrier concentration. Therefore, the amplitude of the 1/*f* noise (α) is attributed to either the amount of carrier scattering or the number of active traps participating in the generation-recombination process within the sample. Thus, α can be used as a figure of merit for material quality. The calculated Hooge parameter for the InGaAs QW device is 1.34×10^{-4}, which is consistent with high quality devices (typically in the $10^{-4} – 10^{-6}$ range) [9].

2.3.3 Deep Level Noise Spectroscopy of InGaAs QW Micro-Hall Device

Deep level noise spectroscopy (DLNS) was shown in [8] to be a method of determining the activation energy and location within the band gap of G-R centers. The first step for DLNS is to measure $S_{V,noise}$ as a function of frequency for various temperatures. Averages about chosen frequencies are used to identify $S_{V,noise}$ as a function of temperature. The applied voltage dependency of $S_{V,noise}$ is removed by being divided by V^2, which yields temperature dependent spectral noise density (S_{noise}) for various frequencies and is shown in Fig. 14. Peaks in S_{noise} due to G-R centers shifted toward higher temperatures for increasing frequencies. The two peaks in Fig. 14 indicated two active electron traps [8].

The activation energy (E_1) and possibly the location of the trap within the band (E_0) can be extracted from further analysis of the peaks shown in Fig. 14 as explained in Section 1.5.2. Fig. 15 shows plots of $1/kT_{Max}$ (Fig. 15 (a)) and $\ln(S_{Max})$ (Fig. 15 (b)) as a function of $\ln(\omega)$ for the

peak found between 150 K and 250 K. E_1 for this defect was 0.4 eV. E_0 could not be determined due to the slope of Fig. 15 (b) being close to unity [8].

The same process explained above was carried out for the peak noise density that was found for temperatures greater than 250 K and is shown in Fig. 16. From Fig. 16 (a), E_1 was found to be 0.57 eV. E_0 remained undetermined due to the slope shown in Fig. 16 (b).

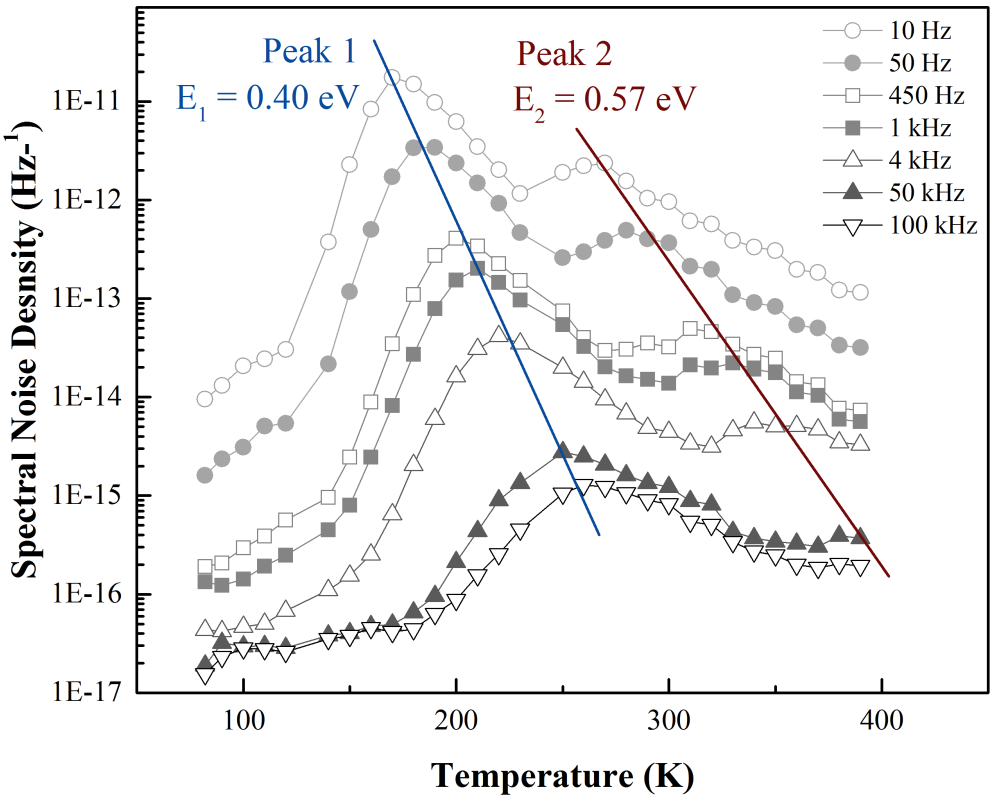

Fig. 14. Spectral noise density as a function of temperature for various frequencies for sample SE210.

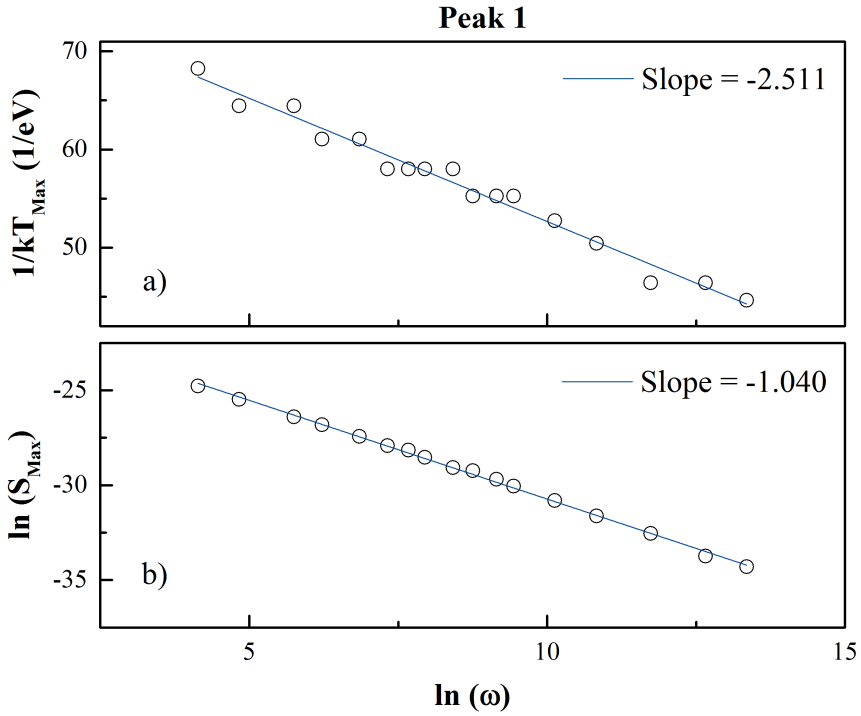

Fig. 15. (a) 1/kT and (b) ln (S_{max}) as a function of ln (ω) for the peak found between 150 K and 250 K for SE210.

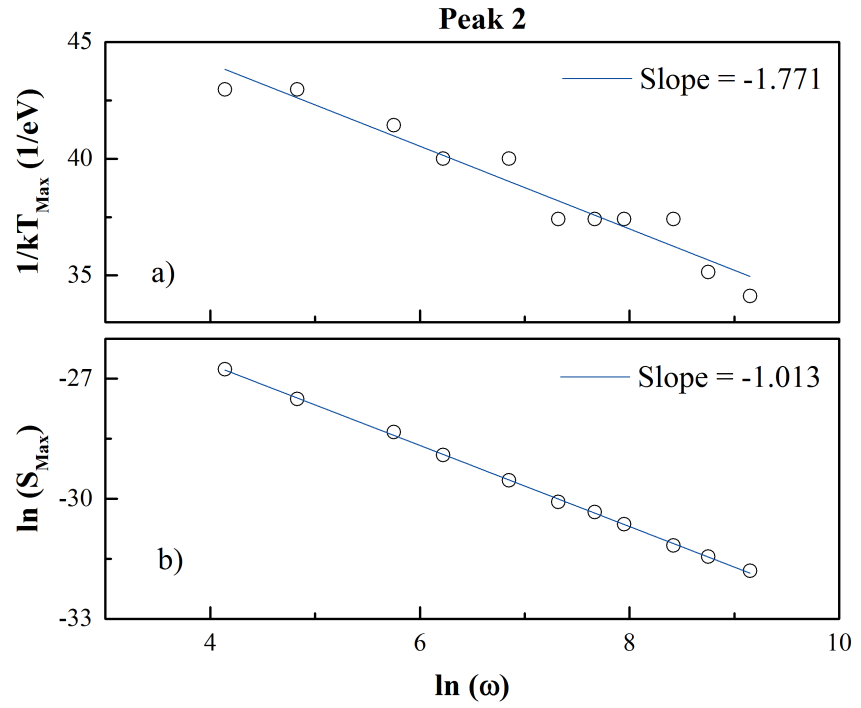

Fig. 16. (a) 1/kT and (b) ln (S_{max}) as a function of ln (ω) for the peak found at temperatures higher than 250 K for SE210.

2.3.4 InGaAs QW Micro-Hall Device Linearity

Hall voltage for sample SE210 as a function of magnetic field for constant bias voltage condition is shown in Fig. 17 for temperatures of 80 K (Fig. 17 (a)) and 390 K (Fig. 17 (b)). The Hall voltage versus magnetic field is also shown for sample SE210 under constant bias current condition for 80 K and 390 K in Fig. 18 (a) and Fig. 18 (b) respectively. The device output voltage remained linear ($R^2 = 0.99$) for these conditions. Device linearity is essential for current prediction based on changing magnetic fields [3].

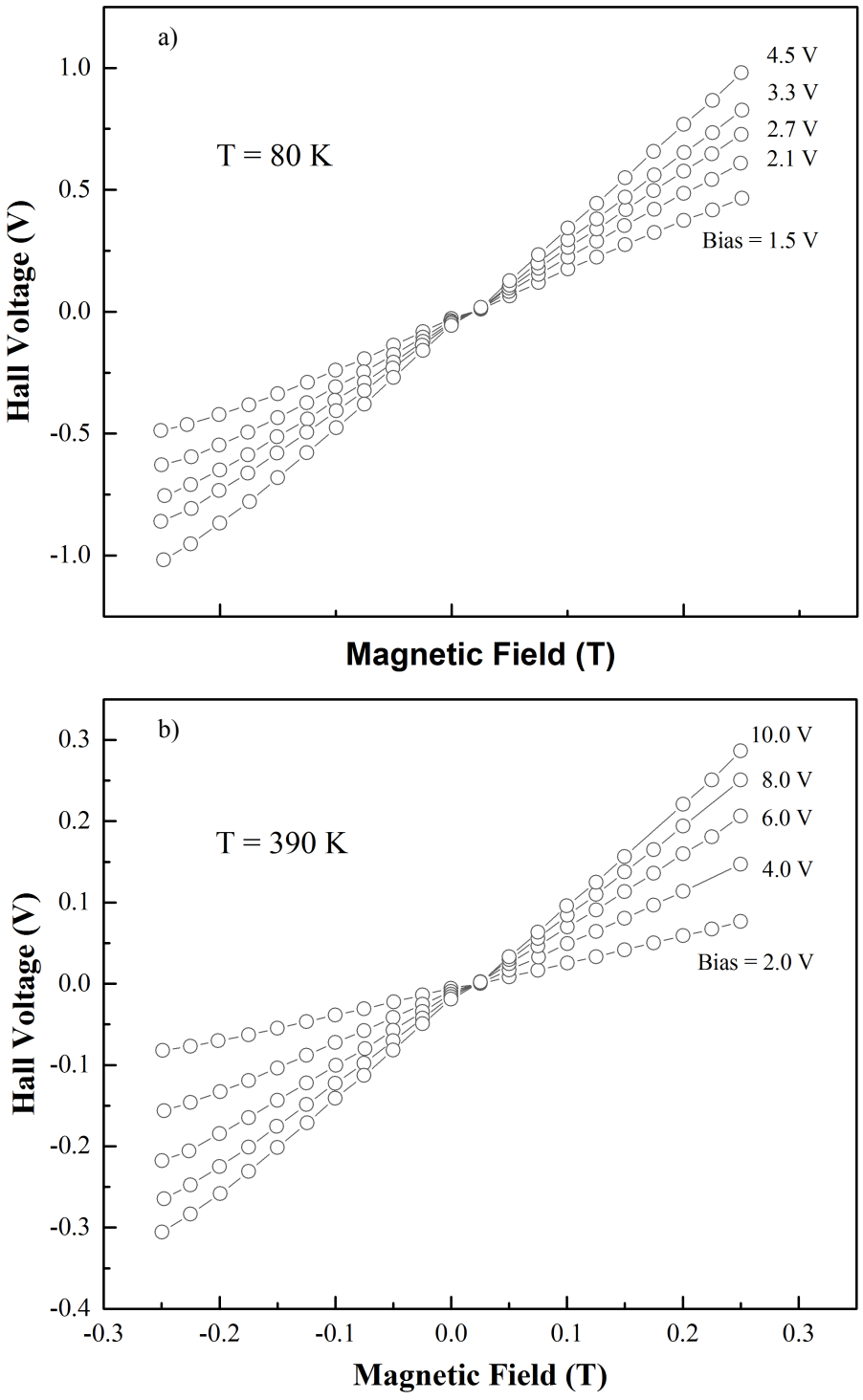

Fig. 17. Hall voltage as a function of magnetic field for sample SE210 under constant bias voltage condition at (a) 80 K and (b) 390 K.

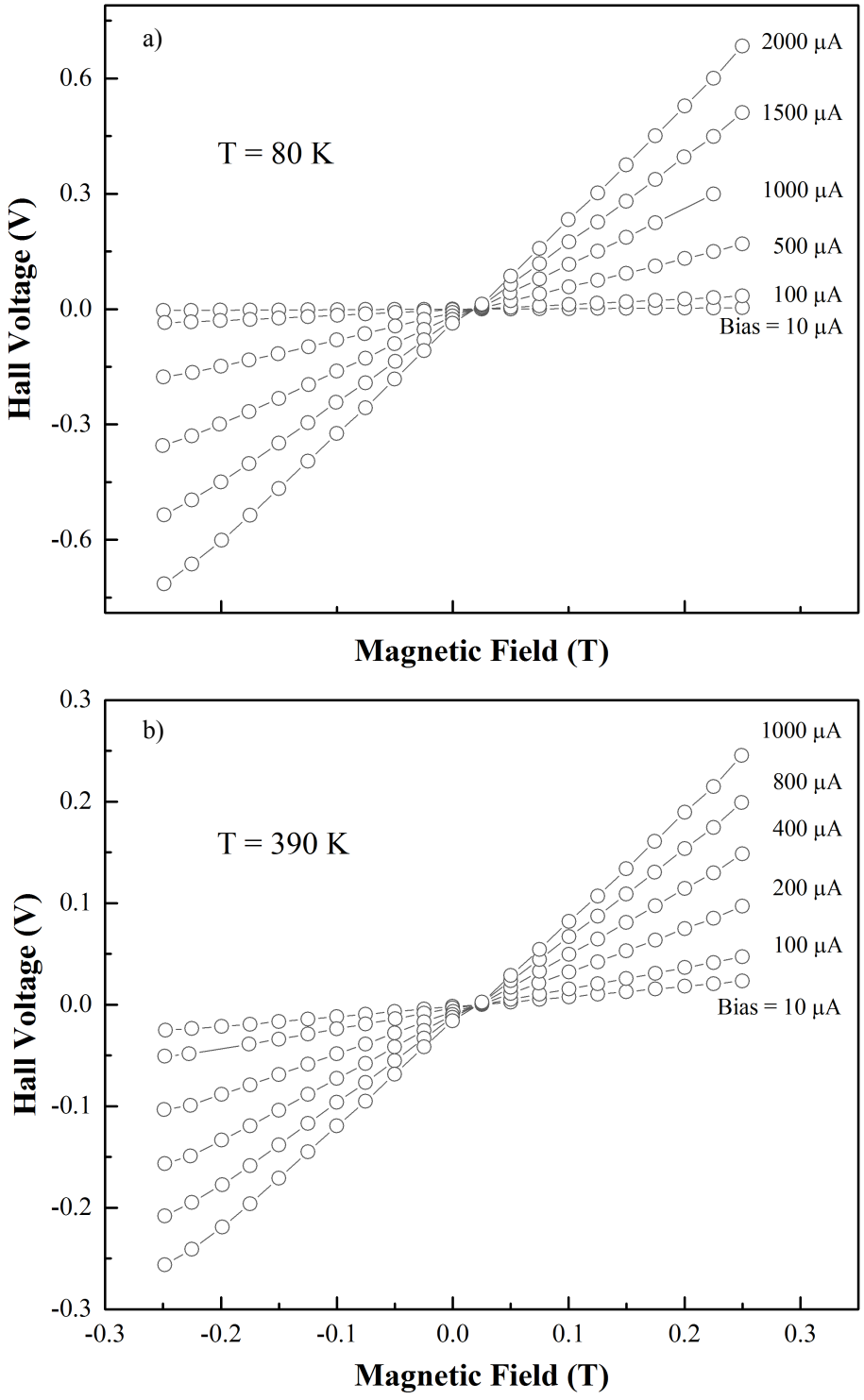

Fig. 18. Hall voltage as a function of magnetic field for sample SE210 under constant bias current condition at (a) 80 K and (b) 390 K.

2.3.5 InGaAs QW Micro-Hall Device Sensitivity.

Absolute sensitivity (S_A) is a measure of the Hall voltage in response to a change in magnetic field (discussed in Section 1.5.3). In other words $S_A = \Delta V_H/\Delta B$, i.e., the slope of data plotted in Fig. 17 and Fig. 18. S_A as a function of different biasing conditions is shown in Fig. 19. From Eq. 12, $V_H \sim \mu V_A$ with constant W/L and B. Considering the relationship between mobility and electric field ($\mu = v/E$ where v is the carrier velocity), the absolute sensitivity of the device should follow velocity-voltage characteristics, which is shown in Fig. 19 (a).

From Eq. 14, $V_H \sim I/n$. I/n increases with increasing electron velocity. The electron velocity will rise with an increase in applied current [5]. Therefore, S_A should increase linearly as a function of bias current. This trend is shown in Fig. 19 (b) as $R^2 = 0.999$ for both 80 K and 390 K.

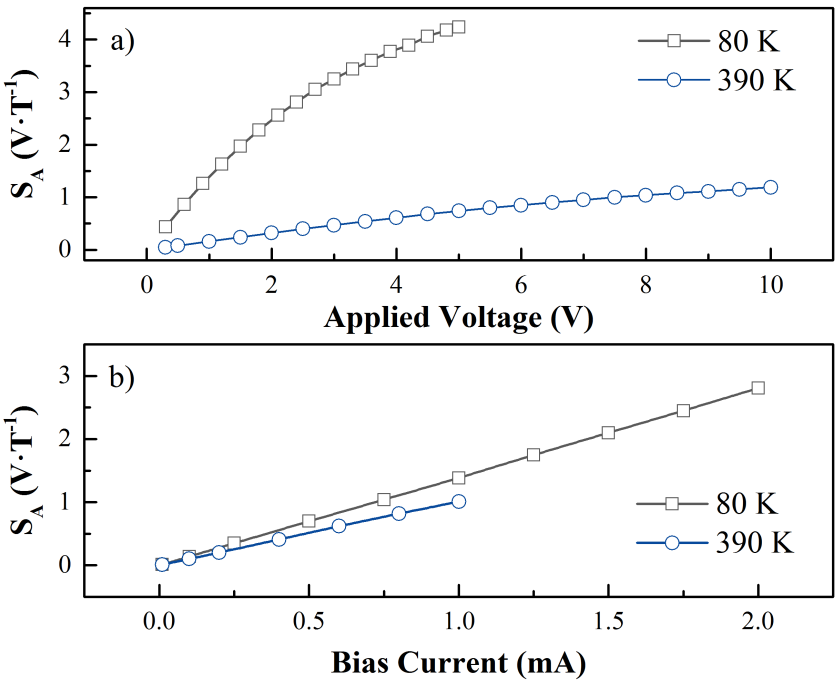

Fig. 19. Absolute sensitivity as a function of (a) applied voltage and (b) bias current for sample SE210.

The efficiency of the device does not very significantly between being operated in constant voltage or constant current modes. The absolute sensitivity with an applied voltage of 5 V recorded for the InGaAs QW micro-Hall device was 4.24 V/T and 0.74 V/T at 80 K and 390 K, respectively. The absolute sensitivity measured for the same structure with a bias current of 1 mA was 2.81 V/T and 1.01 V/T, respectively.

Absolute sensitivity for sample SE210 was measured as a function of temperature and is shown in Fig. 20 for the biasing conditions of 2.5 V (Fig. 20 (a)) and 511 μA (Fig. 20 (b)). These biasing conditions allowed for a high output voltage while maintaining safe operating conditions over a wide temperature range. There was a severe degradation (59% decrease) in device performance from 500 K to 550 K. Under the constant voltage condition, S_A is very small (less than 17% of the 80 K value) for temperatures greater than 350 K. The rapid decrease in S_A in Fig. 20 (b) is due to a sharp increase in carrier density and dramatic decrease in mobility, which can be seen by substituting Eq. 12 and Eq. 13 into Eq. 37. The absolute sensitivity for the InGaAs QW micro-Hall device was found to be 0.70 V/T, 0.60 V/T, and 0.13 V/T for 80 K, 290 K, and 540 K respectively.

The supply voltage related sensitivity (SVRS) and the supply current related sensitivity (SCRS) show magnetic sensing performance under different injection conditions. SVRS and SCRS are calculated using Eqs. 38 and 39 respectively. From Fig. 21 (a), SVRS was seen to reflect mobility behavior under high electric fields. SCRS, however, remained stable (5% change for SCRS verses a 27% change for SVRS) as shown in Fig. 21 (b). For this reason, the mode of operation most suitable for the InGaAs micro-Hall device is constant current mode. The sensitivity remained high (~ 1000 $VA^{-1}T^{-1}$) at temperatures up to 390 K.

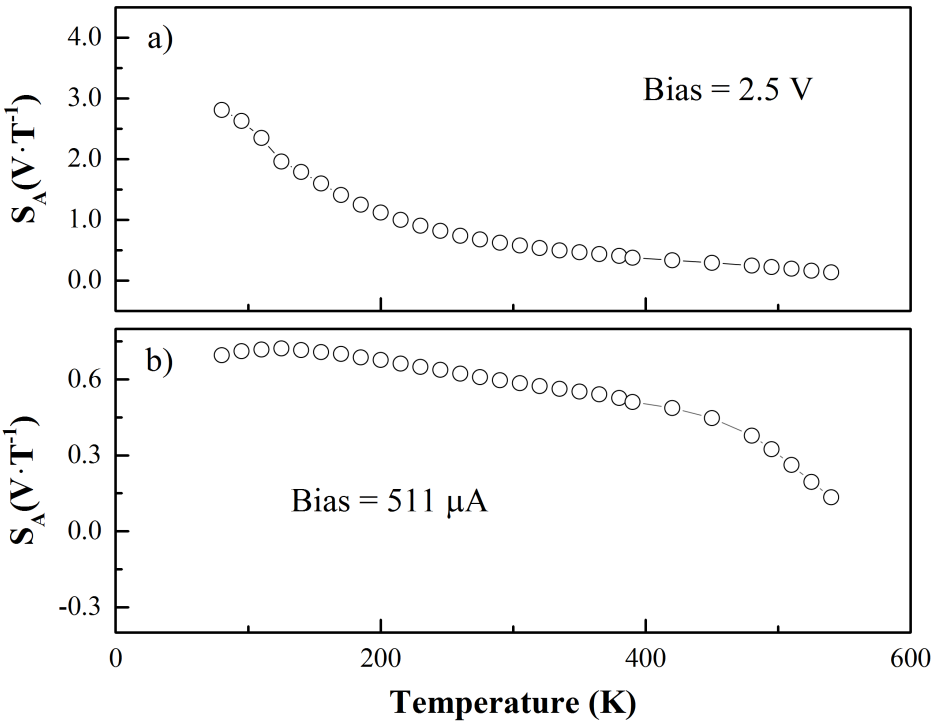

Fig. 20. Absolute sensitivity for Sample SE210 as a function of temperature for (a) constant applied voltage and (b) bias current conditions.

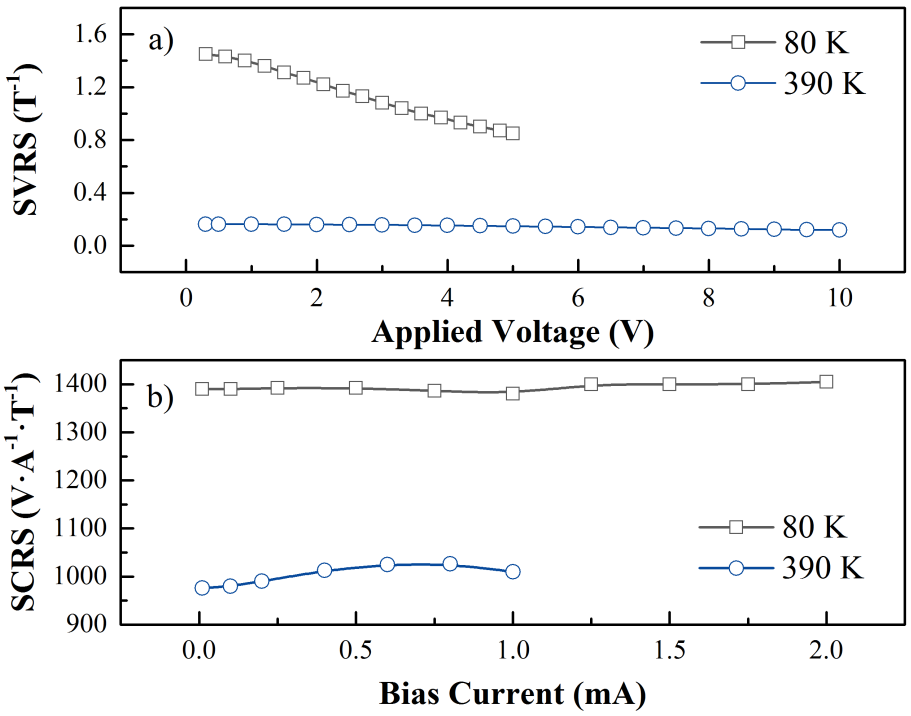

Fig. 21. (a) Supply voltage and (b) Supply current related sensitivity for SE210.

2.3.6 InGaAs QW Device Detection Limit

The detection limit (B_{DL}) is the minimum magnetic field that is detectible by the Hall sensor and is shown in Fig. 22. B_{DL} is the relationship between sensitivity and noise as given by [3]

$$B_{DL} = \frac{\sqrt{S_{noise}\,\Delta f}}{S_A}, \tag{42}$$

where Δf is the sampling width equal to 1 Hz for measurements taken for this project.

Peaks in the detection limit seen in Fig. 22 were due to defects within the device. As seen in Fig. 20 (b), S_A remained relatively stable (decreased by 26.5%) at temperatures between 80 K and 400 K. Therefore, increases in noise caused by active traps (see Fig. 14) resulted in the degradation of B_{DL}. However, the detection limit did remain low (less than mT) over the temperature range of 80 K to 390 K reaching a minimum of 2.5 × 10^{-9} T at 80 K and 100 kHz. The detection limit is highest at 4.4 × 10^{-6} T for 150 K and 10 Hz.

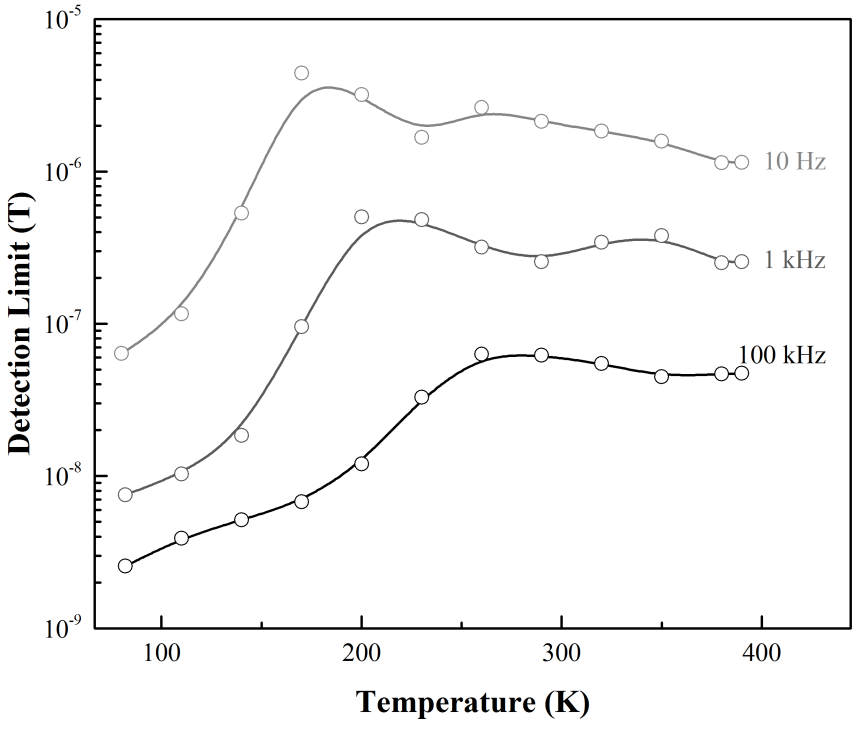

Fig. 22. Detection limit for Sample SE210 as a function of temperature for 10 Hz, 1 kHz and 100 kHz frequencies.

2.4 Summary

Detailed studies of device characteristics of an InGaAs QW micro-Hall sensor made of GaAs/InGaAs/AlGaAs were performed in a wide temperature and frequency range. High device performance was demonstrated, achieving a mobility of 7,800 cm^2/Vs and electron sheet density of 4.2×10^{11} cm^{-2} at room temperature. The InGaAs QW devices with Greek cross geometry (see Section 3.7.4 for Greek cross description) and active area of 40 μm exhibit high absolute sensitivities of 0.70 V/T, 0.60 V/T, and 0.32 V/T for 80 K, 290 K, and 495 K, respectively. At the same time, supply current related sensitivities as high as 1362 V/T/A, and 1168 V/T/A, and 626 V/T/A were found at 80 K, 290 K, and 495 K, respectively. A comparison of sample SE210 to the state of the art magnetic sensitivity and detection limit is shown in Table 2. This device demonstrated excellent linearity ($R^2 = 0.99$) in response to magnetic field at different biases and temperatures.

Table 2. Comparison of Sample SE210 with State-of-the-Art GaAs QW and InGaAs QW Hall Effect Sensors

Property	Units	Ref [11]	Ref [12]	Ref [13]	Ref [14]	SE210
Sturcture	-	GaAs QW	$In_{0.53}Ga_{0.47}As$ QW	InGaAs QW	$In_{0.25}Ga_{0.75}As$ QW	$In_{0.12}Ga_{0.88}As$ QW
Width	mm	0.2	0.2	0.2	0.1	0.04
μ_{Hall} at 300 K	cm2/Vs	13000	16000	15200	8100	7800
n_{2D} at 300 K	cm^{-2}	1.76E+12	2.00E+12	1.41E+12	1.50E+12	4.20E+11
B_{DL}	nT	120	60	1000	60	300
Normalized B_{DL}	nT•mm	24	12	200	6	12

Low frequency noise studies were used as a separate diagnostics tool to estimate device quality based on studies of Hooge parameter. A Hooge parameter of 1.34×10^{-4} was found at room temperature. Applying these noise studies at room temperature the detection limit of the magnetic field was estimated to be 6.2×10^{-8} T. Temperature dependent studies of low frequency noise revealed two electrically active deep traps with activation energies of 0.40 eV and 0.57 eV.

These traps degraded magnetic field detection limit in the temperature ranges of 150 K – 250 K and 330 K – 370 K causing higher noise due to generation-recombination phenomena in the device volume.

Studies of device performance at high temperatures indicate that this type of heterosturcture was applicable and demonstrated a high performance level for temperatures below 500 K. However, for temperatures above 500 K, rapid decrease of electron mobility and increase of electron sheet density required development of a new material system with larger band gap and high electron drift velocities. In the following chapter, GaN/AlGaN systems will be considered as an alternative structure for high temperature applications.

Chapter 3: Development of GaN-Based Micro Hall Devices

There has been a large devotion to GaN-based device research in the last two decades due to the material's wide band-gap, high saturation of electron drift velocity, and high breakdown voltage. In addition, for high temperature Hall effect sensors, GaN offers improved thermal stability and relatively high mobility as compared to GaAs devices [19].

GaN and AlN are polar crystals, which influences the design of GaN based devices. Both the polarization and band offsets must be considered when forming quantum wells out of GaN and AlN. Furthermore, polarization in the AlGaN layer of an AlGaN/GaN structure can be altered as a means for tuning the electron concentration in the two-dimensional electron gas (2DEG) [19], [20].

2DEG formation is also important for Hall sensor design because of the inverse relationship between carrier concentration and device sensitivity of a sensor operating in current biasing mode. In an AlGaN/GaN HEMT structure, the 2DEG forms without doping the barrier. Therefore, no additional ionized donors that reduce mobility are present. However, the choice of substrate properties and AlGaN layer thickness are important factors for further altering the sheet density of the device [19], [20], [21], [22].

In the following sections GaN properties will first be described, followed by an explanation of polarization. Next a discussion of 2DEG formation as well as sources of electrons is given. The basic principles of MBE will be explained followed by the growth process and growth parameters for GaN HEMT structures. Further details concerning growth are given in Appendix H. Once structures are grown they must be processed. Processing is a critical aspect of GaN device fabrication due to the role of surface states, which will be explained in Section 3.7. The chapter will conclude with characterization results.

3.1 Basic Properties of Wurtzite GaN

GaN is able to crystalize in two different crystal structures, wurtzite (hexagonal) and zinc blende (cubic). Wurtzite is the typical crystal structure of GaN and is also thermodynamically stable whereas zinc blende is metastable [23]. For this project only wurtzite GaN was grown.

The hexagonal crystal structure for GaN and the three lattice parameters a, c, and μ [18] are shown in Fig. 23 (a) [16]. Both wurtzite GaN and AlN have the same crystal structure but slightly different lattice parameters [15]. A list of values for a, c, and μ for GaN and AlN are given in Table 3. For ternary alloy $Al_xGa_{1-x}N$, [24]

$$\beta(Al_xGa_{1-x}N) = x\beta_0(AlN) + (1-x)\beta_0(GaN) \tag{43}$$

where β can be a, c, or μ, and $\beta_0(AlN)$ and $\beta_0(GaN)$ are the unstrained lattice parameters for AlN and GaN respectively.

There are four lattice vectors used to describe the hexagonal crystal structure, which are $\mathbf{a}_1$, $\mathbf{a}_2$, $\mathbf{a}_3$, and $\mathbf{c}$ (Fig. 23 (b)) [25]. The c – plane and a – plane are shown for clarity in Fig. 23 (c) and (d) respectively. All samples were grown in the [0001] direction for which there are two types of GaN growth variations, Ga terminated and N terminated. For this project only Ga terminated growth is considered.

The energy gaps (E_G) for GaN and AlN are 3.51 eV and 6.25 eV respectively. It has been shown experimentally that bowing is to be considered when calculating E_G for ternary III-nitride alloys. E_G for $Al_xGa_{1-x}N$ is therefore given by [22]

$$E_G(Al_xGa_{1-x}N) = xE_G(AlN) + (1-x)E_G(GaN) + x(1-x)C \tag{44}$$

where C is a bowing parameter equal to 0.7 (Γ-valley) for AlGaN. A graph of E_G as a function of a is shown in Fig. 24.

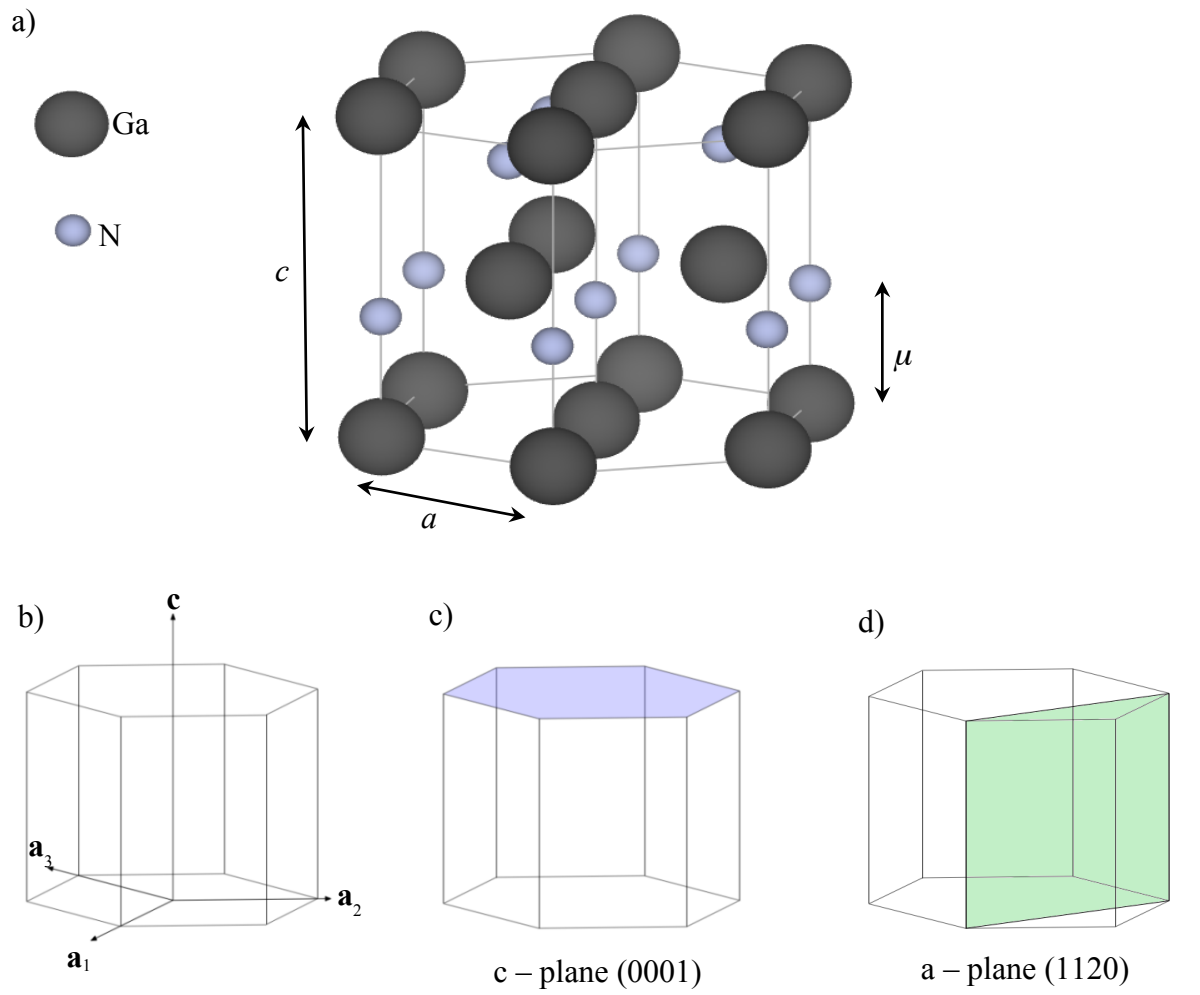

Fig. 23. (a) Hexagonal crystal structure of GaN, μ is in units of *c*. (b) Lattice vectors. (c) c-plane. (d) a-plane.

Table 3. Band Parameters for GaN and AlN

Parameters	Units	GaN	AlN	Ref
E_G	eV	3.51	6.25	[26]
a_0	Å	3.189	3.112	[26]
c_0	Å	5.185	4.982	[26]
μ_o	c	0.376	0.380	[27]
e_{31}	C/m^2	-0.49	-0.60	[27]
e_{33}	C/m^2	0.73	1.46	[27]
c_{13}	GPa	106	108	[26]
c_{33}	GPa	398	373	[26]
P_{SP}	C/m^2	-0.034	-0.090	[26]

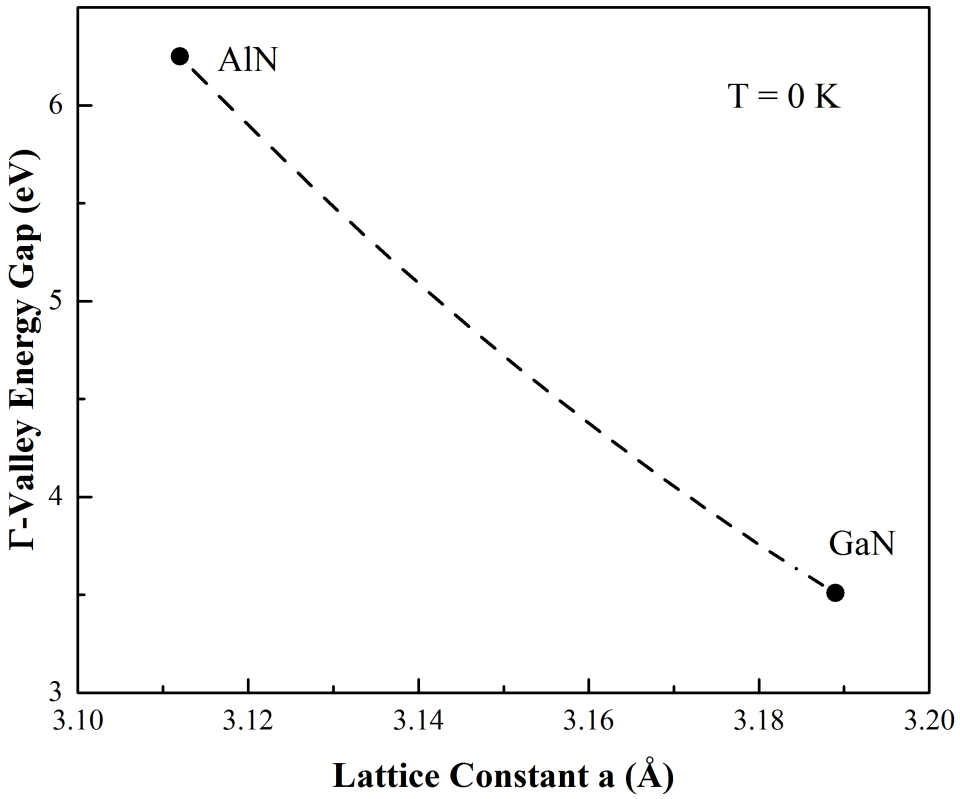

Fig. 24. Energy band gap (Γ-valley) as a function of lattice constant *a* for AlN, GaN, and AlGaN.

3.2 Polarization within GaN/AlGaN Material Systems

An important part of understanding the AlGaN/GaN system is to understand polarization and the source of the two dimensional electron gas (2DEG) at the heterojunction. The difference in polarization from GaN to AlGaN results in a net bound charge located at the AlGaN interface. The bound charge has a large influence on the band structure [28]. In this section, a description is given of polarization, quantum well formation, and the source of the 2DEG in AlGaN/GaN HEMT structure.

3.2.1 Spontaneous Polarization

The 2DEG formation in an AlGaN/GaN structure is due to both the band offset and an abrupt change in polarization at the AlGaN-GaN junction. III-nitrides are polar crystals due to the distribution of charge within the constituent atoms and the symmetry of the crystal [28]. The magnitude of the polarization field increases from GaN to AlN (for hexagonal crystal structure), which is due to the difference in bond lengths (μ) and lattice constants (a and c). The polarization that is dependent on these structural parameters is called the spontaneous polarization ($\boldsymbol{P}_{sp}$) [28]. Below, two approaches for determining $\boldsymbol{P}_{sp}$ are described. The first approach is strictly a geometrical argument while the second approach is simply averaging experimental data. Both will be described here as the geometrical approach allows for a good visualization and averaging approach is arguably more accurate. However, there is still a discrepancy in method two as many different values for $\boldsymbol{P}_{sp}$ have been found through experiment.

For the geometrical argument, consider the point charge model shown in Fig. 25. By summing the vector location of the atoms, the dipole moment for this system is found to be [25]

$$p_{dipole} = e^{*}c(\mu - 3/8). \tag{45}$$

where e^{*} is the effective charge of the cation. Dividing the dipole moment by the volume, the polarization is found to be [29]

$$P_{SP} = \frac{4e^{*}(3/8-\mu)}{a^{2}\sqrt{3}}. \tag{46}$$

While Eq. 46 is based on a simplified model, one can still see the effect that μ and a have on this system when changing form AlN (AlGaN) to GaN. Using Eq. 46, e^{*}(GaN) and e^{*}(AlN) values of 4.277 × 10^{-19} C and 4.245 × 10^{-19} C respectively [30], and the values for a and μ given in Table 3, P_{SP}(GaN) is found to be -0.015 C/m^2 while P_{SP}(AlN) is found to be -0.076 C/m^2.

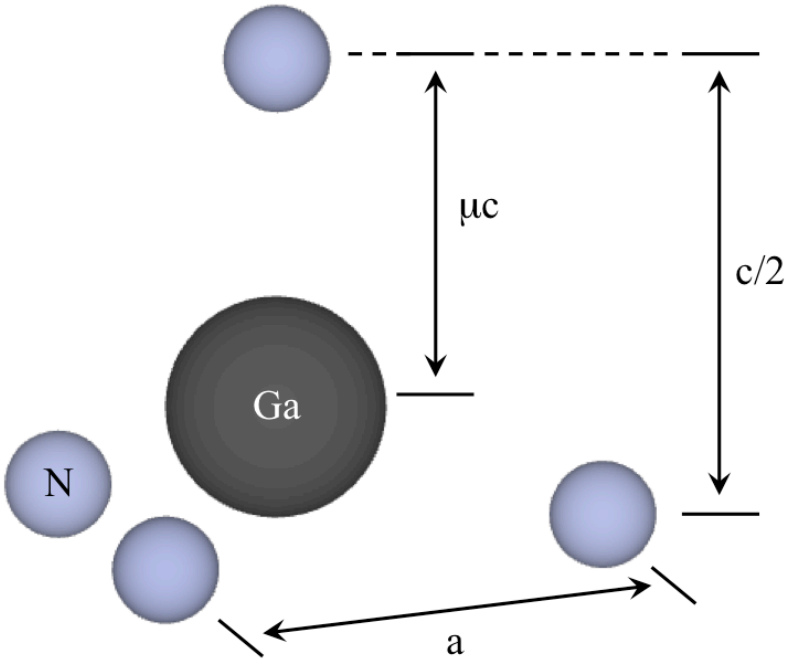

Fig. 25. Point charge model for GaN showing μ, a, and c.

Another approach to calculate P_{SP} is to use the values given in Table 3 along with the following equation [26]:

$$P_{SP}(Al_xGa_{1-x}N) = xP_{SP}(AlN) + (1-x)P_{SP}(GaN) + x(1-x)C \tag{47}$$

where the bowing parameter *C* is -0.021 for AlGaN [26]. The problem with this method is there have been several different values for P_{SP} calculated. These values along with the calculations from both approaches described above for determining P_{SP} are shown in Table 4.

Table 4. Variations in P_{SP}(GaN) and P_{SP}(AlN)

Source	P_{SP}(GaN) [C/m^2]	P_{SP}(AlN) [C/m^2]
Eq. 46	-0.015	-0.076
Ref. [26]	-0.034	-0.090
Ref. [27]	-0.029	-0.081

3.2.2 Piezoelectric Polarization

When AlGaN is strained on GaN, the AlGaN layer is under tensile strain in the ***a*** direction and compression strain in the ***c*** direction. Again, due to the crystal symmetry, the strain results in an induced polarization. The strain-induced polarization is called piezoelectric polarization ($\boldsymbol{P}_{PZ}$). The magnitude of $\boldsymbol{P}_{PZ}$ in the [0001] direction is given by [28]

$$P_{PZ} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y) \tag{48}$$

where e_{31} and e_{33} are piezoelectric coefficients, $\epsilon_z = (c - c_0)/c_0$, and $\epsilon_x = \epsilon_y = (a - a_0)/a_0$ due to the *a* parameter being constant in the x-y plane. Using the relation [28]

$$\frac{c-c_0}{c_0} = 2\frac{C_{13}}{C_{33}}\frac{a-a_0}{a_0} \tag{49}$$

and Eq. 48, P_{PZ} can now be written as [28]

$$P_{PZ} = 2\frac{a-a_0}{a_0}\left[e_{31} - e_{33}\left({}^{C_{13}}/_{C_{33}}\right)\right], \tag{50}$$

where c_{13} and c_{33} are elastic constants.

Again, for the AlGaN/GaN HEMT structures grown for this project, the AlGaN layer was strained. Therefore, a_0, e_{31}, e_{33}, c_{13}, and c_{33} for AlGaN should be used in Eq. 50. Linear fits can

be used for calculating the correct AlGaN parameter values for a given Al percentages. Since AlGaN is strained to GaN, a(GaN) should be used.

3.3 Bound Charge located at the GaN-AlGaN Junction

The difference in polarization at the AlGaN-GaN junction is given by [19], [28]

$$\Delta \boldsymbol{P} = \boldsymbol{P}_{SP,AlGaN} + \boldsymbol{P}_{PZ,AlGaN} - \boldsymbol{P}_{SP,GaN}. \tag{51}$$

From the polarization, the net bound charge at the junction can be calculated by [4]

$$\sigma_{bound} = \Delta \boldsymbol{P} \cdot \boldsymbol{n}. \tag{52}$$

Using Eqs. 47, 51, and 52 along with the value of $\boldsymbol{P}_{SP,GaN}$ given in Table 1, σ_{bound} was calculated for x = 0.30, 0.20, and 0.15. The results are given in Table 5 and are in agreement with simulations shown in Fig. 26.

Reducing the Al concentration will reduce the sheet density by reducing both $\boldsymbol{P}_{SP,AlGaN}$ and $\boldsymbol{P}_{PZ,AlGaN}$ [19]. Reduction of sheet density by decreasing Al molar fraction in the AlGaN layer is shown in Fig. 26 [18] and by comparing NH64 with NH63 (results given in Section 3.8).

Table 5. Spontaneous Polarization, Piezoelectric Polarization, and Bound Charge for AlGaN/GaN Structures with Different Al Molar Fractions in the AlGaN Layer

x	P_{SP} (C/m^2)	P_{PZ} (C/m^2)	σ_b(cm^{-2})
0.3	-0.0464	-0.0114	1.49E+13
0.2	-0.0418	-0.0073	9.43E+12
0.15	-0.0397	-0.0050	6.68E+12

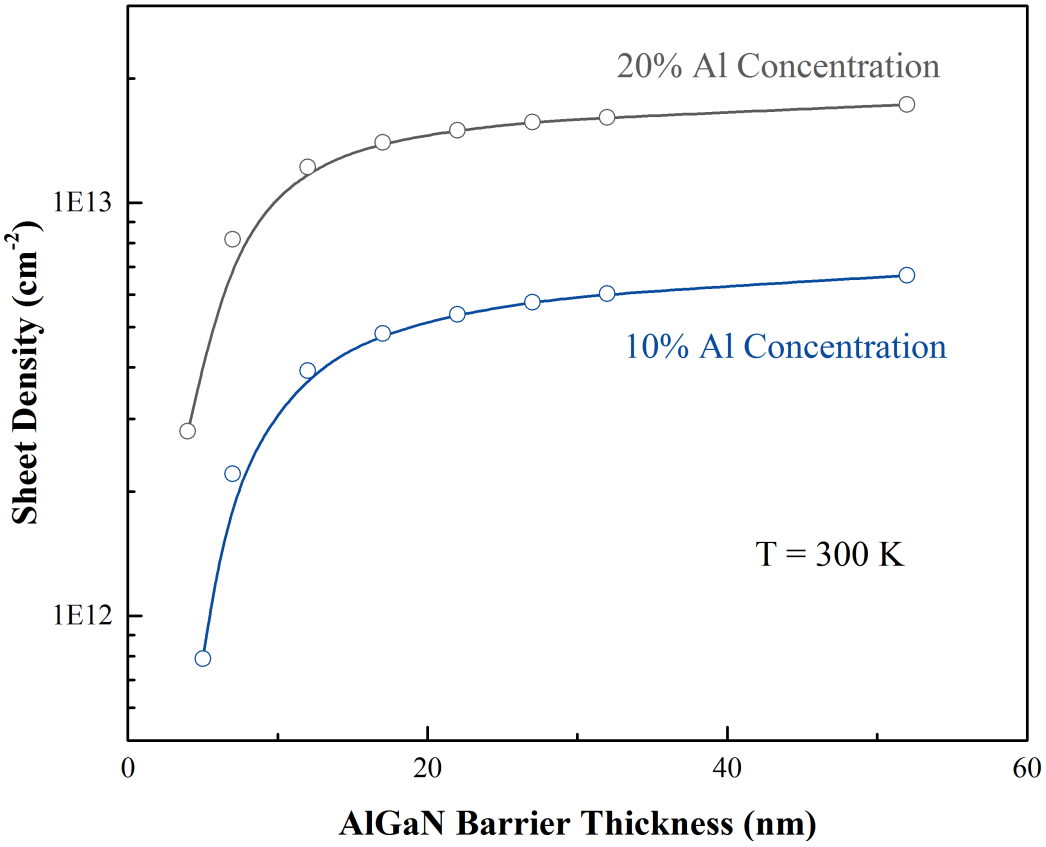

Fig. 26. Sheet density as a function of AlGaN barrier thickness and Al molar fraction. (simulated by [18]).

3.4 Heterojunction Formation and Sources of 2DEG in GaN/AlGaN System

The sheet of positive bound charge at the junction creates an electric field, which can be calculated by [4]

$$\boldsymbol{E} = \frac{\Delta \boldsymbol{P}}{\epsilon_0 \chi_0} \tag{53}$$

where ϵ_0 is the permittivity of free space and χ_0 is the electric susceptibility. The calculated electric field for x = 0.20 was ~ 1x10^8 V/m. This high electric field at the AlGaN-GaN junction can have a large influence on the band structure, creating the triangular quantum well at the heterojunction, which was at a depth of 25 nm in this case (see Fig. 27). The slope of the bands in the $Al_{0.2}Ga_{0.8}N$ layer was due to the electric field across it. An electric field in the opposite

direction was found in the GaN cap layer due to the bound negative charge at the surface [31]. The Schottky barrier height at the surface was estimated by [28]

$$e\phi_b(x) = 1.3x + 0.84 \text{ (eV)}. \quad (54)$$

Free electrons that fill the well creating a 2DEG can be supplied by donor states in GaN template, buffer or from the surface [20]. Evidence from experimental results of the contribution of electrons from the GaN template is given in Section 3.8.

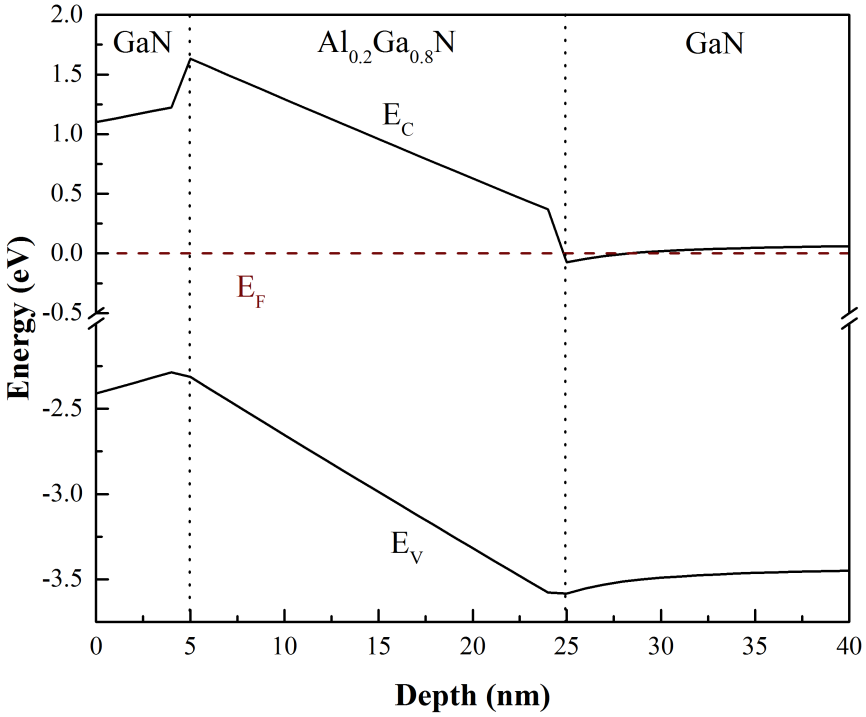

Fig. 27. Band structure of a GaN/$Al_{0.2}Ga_{0.8}$N/GaN HEMT device simulated by [18].

3.5 Sheet Density and Mobility Studies for GaN/AlGaN HEMT Structures

Changes in the AlGaN barrier thickness also have a large effect on sheet density, especially in the 2 – 10 nm range. This is due to the electrons that are attracted to the surface screening the electric field that is created by the bound positive charge in the AlGaN layer near the AlGaN barrier and GaN buffer interface. The screening lowers the electric field at the heterojunction

causing the QW to be very shallow. As barrier thickness increases, the screening effect is reduced and the well is deepened [20]. This effect has been simulated and the results are shown in Fig. 26 where the sheet density increases with barrier thickness. The sheet density reaches saturation at σ_{bound}, Eq. 52.

Evidence of electron screening can also be seen in Fig. 28 where the well depth and E_0 are shown. An unintentionally doped (UID) substrate is assumed. The Fermi level remains constant as a function of barrier thickness due to the large amount of donors at the surface [20]. However, the well depth increases by 15 meV as the barrier height increases from of 10 nm to 20 nm resulting in the increased population of E_0 as it falls below the Fermi level.

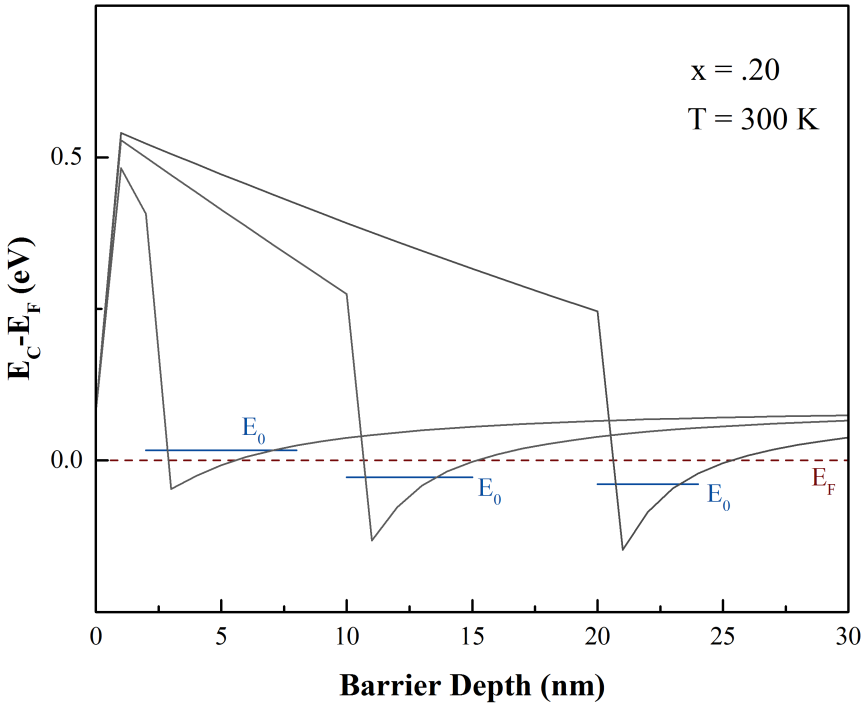

Fig. 28. Conduction band edge as a function of barrier thickness [18].

It has been shown by [20] and [28] that decreasing aluminum composition within the AlGaN barrier increases mobility at temperatures below 150 K. This is likely due to a reduction of alloy scattering. As shown in Fig. 29, the wave function penetrates the AlGaN layer. Reducing the

number of random Al atoms in the AlGaN layer will reduce this type of scattering and increase mobility. Alloy scattering has a strong dependence on carrier concentration [32]. However, at temperatures above 150 K, phonon scattering is dominant and hides the role of alloy scattering [20].

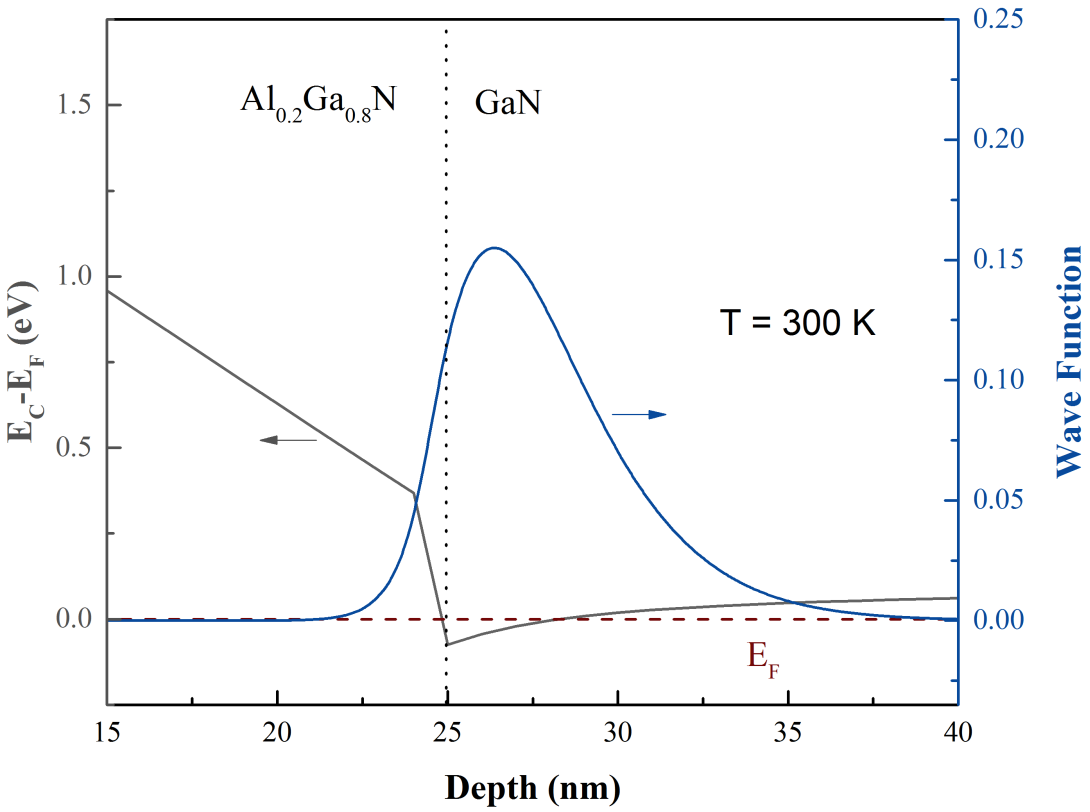

Fig. 29. Conduction band edge and wave function as a function of depth for an $Al_{0.2}Ga_{0.8}N$ structure.

Another method that has been shown to increase mobility is to add a thin (~ 1 nm) AlN layer between the GaN buffer and AlGaN barrier [33]. The increased barrier height at the GaN/AlN interface blocks carriers in the 2DEG from entering the AlGaN layer. This is shown in Fig. 30 were the wave function penetration into the AlGaN layer is decreased for the sample with an

AlN layer, thus reducing alloy scattering and increasing mobility. The AlN layer must remain thin in order to prevent lattice relaxation. Wosko *et al* studied Hall mobility as a function of AlN barrier thickness. The result was an optimal thickness of 1.3 nm [33].

In practice, however, the Hall measurement results for the growth of this GaN/AlN/AlGaN structure was not as expected and resulted in a decrease in mobility as compared to samples without the AlN layer. This was most likely due to roughness at the GaN/AlN interface. More research is needed in order to effectively utilize the AlN barrier in this system.

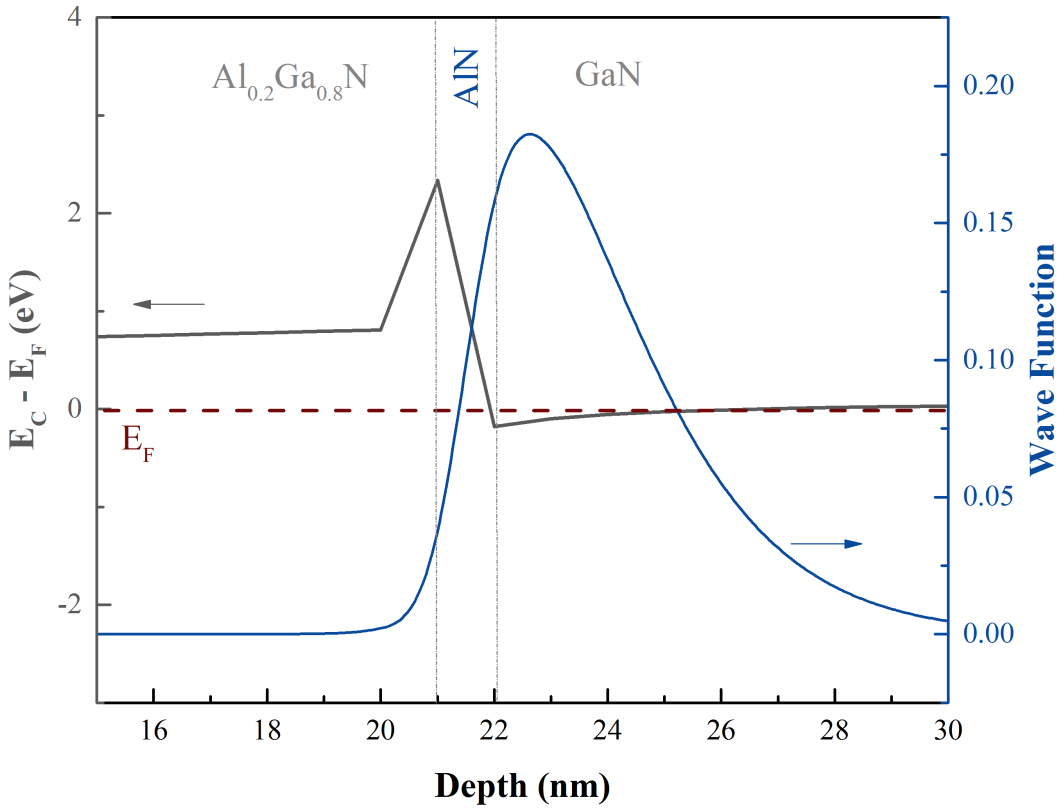

Fig. 30. Conduction band edge and wave function vs. depth for GaN/AlGaN/GaN and GaN/AlN/AlGaN/GaN structures.

3.6 Growth of GaN-Based Structures by MBE

The three major epitaxial growth methods that are used are:

1. hybrid vapor phase epitaxy (HVPE)
2. metal organic chemical vapor deposition (MOCVD)
3. molecular beam epitaxy (MBE).

HVPE offers very fast growth rates (100 μm/hr) and can produce high quality (dislocation density ~10^7), large diameter layers. MOCVD is used in industry because of the ability to produce high growth rates, high quality layers, and in-situ thickness monitoring. However, in the research field MBE is often the preferred method of GaN epitaxial growth because of the added benefit of in-situ characterization (most notably growth rate and composition). MBE is a good way to reduce interface roughness in heterostructures [34]. MBE was the growth method used for this project and will be discussed in this chapter along with the parameters used for growth of GaN-based micro-Hall devices.

3.6.1 Basic Components of MBE

MBE growth was carried out using a VEECO Gen II MBE system, which is shown schematically in Fig. 31. In this system there were three vacuum chambers. The intro chamber was where the samples were initially loaded and outgassed. The typical pressure post outgas was about 5E-8 Torr. The sample was then transferred to the buffer chamber where a second outgas station was located. The pressure in the buffer chamber was about 1E-10 Torr. While in the buffer chamber, the sample was attached to the transfer arm and loaded on to the sample holder located in the growth chamber. The typical pressure in the growth chamber (while no growth occurs) was 5E-11 Torr.

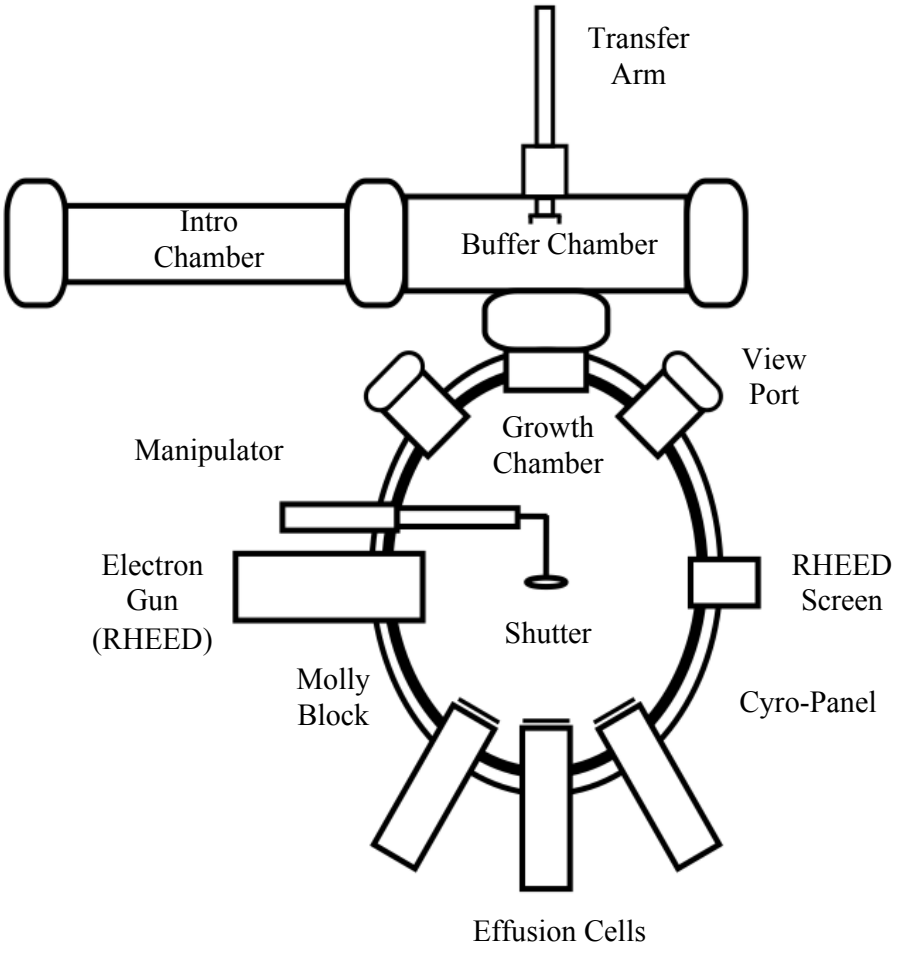

Fig. 31. Top down schematic of the VEECO Gen II MBE System.

The effusion cells housed the metals that were used in growth and were pointed towards the sample holder. For this system the metals were Ga, Al, In, Mg, and Si. Mg and Si were used for p-type and n-type doping respectively. The effusion cells were kept at temperatures well above the metals melting point (350 – 750 °C) during periods of no growth and heated to high temperatures (400 – 1111 °C) during growth. The high temperature during growth caused a pressure of metal vapor to build in the cells. Shutters were then opened to allow the material to reach the sample holder in the form of atomic beams.

Once the sample was loaded onto the sample holder and the growth chamber was sealed, the growth process was carried out. During growth, the sample holder rotated at 5 RPM in order to increase the uniformity of epitaxial growth.

In-situ characterization was carried out by reflective high energy electron diffraction (RHEED). The RHEED system consisted of an electron gun that was pointed towards the sample holder and a phosphorus screen located directly across the chamber (see Fig. 31). A diffraction pattern resulted from the coherent scattering of the electrons from the substrate's surface atoms formed on the RHEED screen and was then transferred to a computer where the diffraction pattern and intensity was measured.

The growth rate is one growth parameter that can be measured by RHEED. The growth rate can be found by recording the changes in intensity over time. If the surface of the sample is smooth, the intensity of RHEED will be high (Fig. 32 (a)). As atoms are deposited on the surface of the sample, there will be a disorder about them. The disorder will cause scattering of electrons and therefore low measured intensity (Fig. 32 (b)). As a monolayer is completed the surface disorder will decrease and the measured intensity will rise which is shown in Fig. 32 (c). The RHEED recovery time (time from Fig. 32 (a) to Fig. 32 (c)) is the time for one monolayer of material to form and thus can be converted to a growth rate in "thickness per unit time"

Information about surface morphology can also be gained from RHEED. In real space, a smooth surface (2D growth) translates to a "streaky" RHEED pattern. A rough surface (3D growth) is shown by a "spotty" RHEED pattern. Streaky and spotty are two terms that are often used when describing RHEED patterns. A streaky RHEED image from GaN growth is shown in Fig. 33. For GaN growth a spotty RHEED image usually indicates growth in the N-rich regime. By experiment, N-rich growth results in rough surfaces [35].

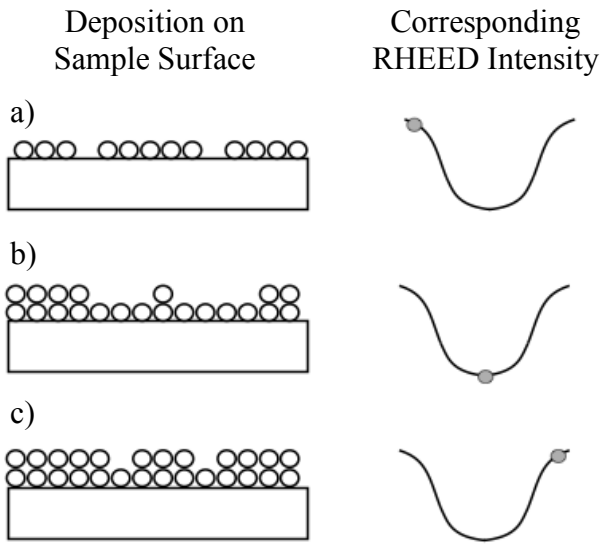

Fig. 32. Surface morphology and RHEED intensity.

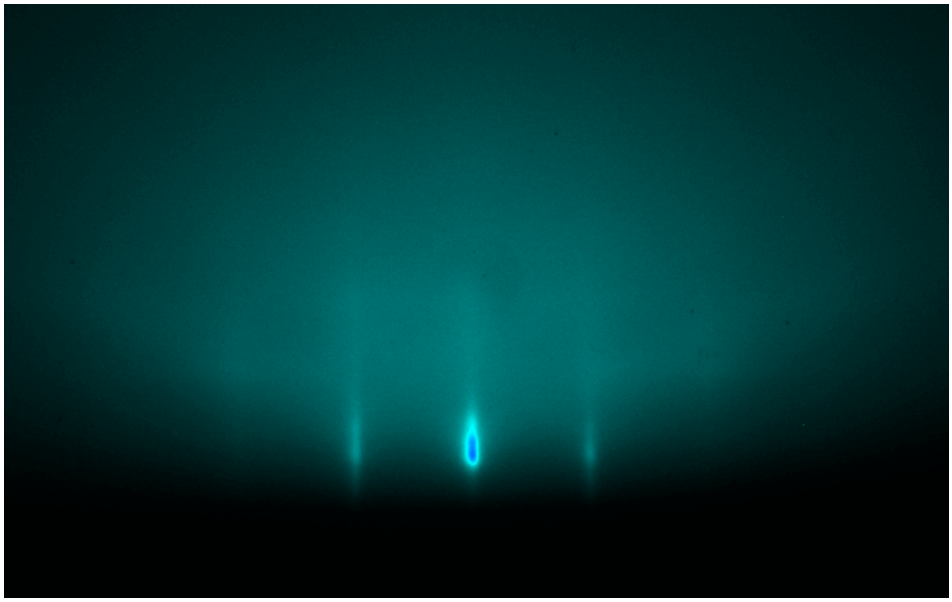

Fig. 33. "Streaky" RHEED image captured during GaN Growth.

3.6.2 Growth Calibrations

One growth calibration that should be performed periodically is finding effusion cell temperature as a function of Beam Equivalent Pressure (BEP). This allows for the determination of the appropriate effusion cell temperature needed in order to achieve different molar fractions in alloys. An example of the relationship of cell temperature and BEP is shown in Fig. 34 for Ga. In order to make this measurement, the beam flux monitor (BFM in Fig. 31) was rotated to a position facing the effusion cells. The BFM is actually an ion gauge that measures pressure. From the pressure, the BEP was calculated. After the BEP was recorded for an adequate effusion cell temperature range, the data were fit by

$$y = A_0 + A_1 \ln(x) \tag{55}$$

where A_0 is 1754.509 and A_1 is 54.025 for the base of the Ga cell. In the case of Ga, Eq. 55 was typically used to estimate the Ga effusion cell temperature needed in order to achieve a Ga rich growth condition that was 2% over the stoichiometric point.

Calibrating the Al molar fraction deposited in the AlGaN layer was a critical step in device fabrication. As shown in Fig. 26, the electronic properties of the device vary greatly (about 70% change) for Al molar fractions between 10 % and 20 %. Three samples were grown (three points at the highest Al concentration in Fig. 34) in order to find a linear trend line that was used to estimate the Al concentration. More data was collected and the following equation was used

$$Al\% = B_0 + B_1 exp\left(\frac{T_{Al,Base}}{t_1}\right), \tag{56}$$

where B_0, B_1, and t_1 are given in Table 6. This data will be used for further growths with varying Al concentrations.

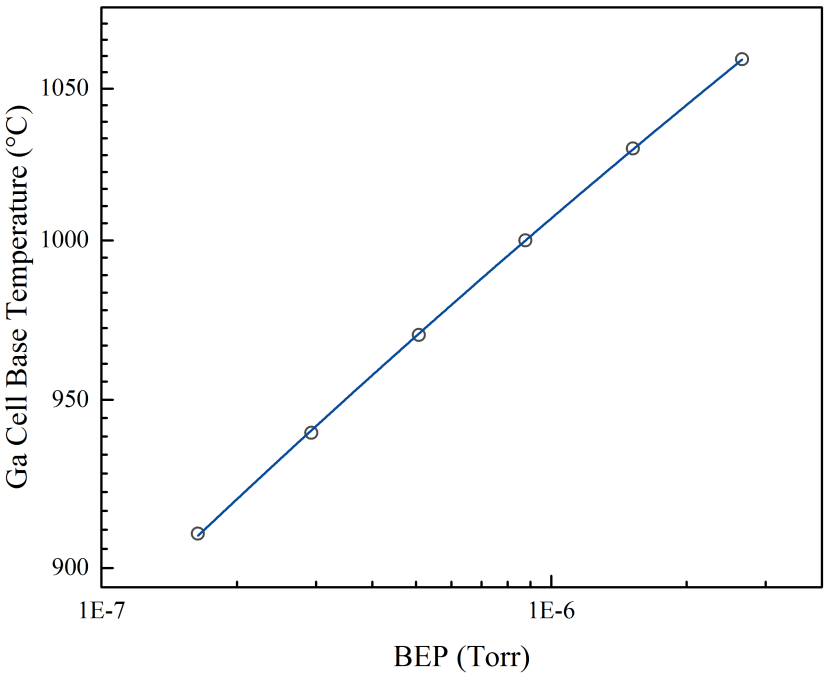

Fig. 34. Ga cell base temperature as a function of BEP.

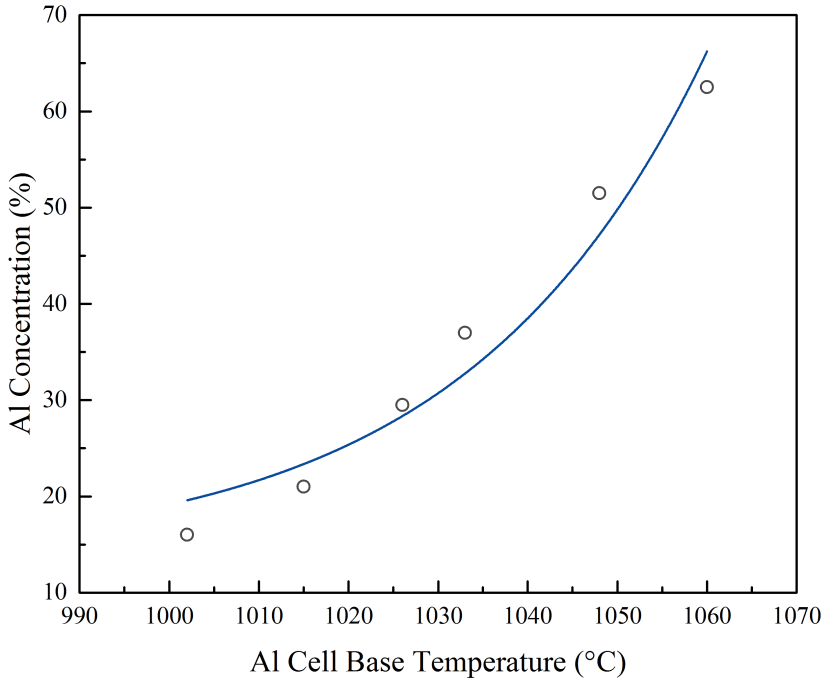

Fig. 35. Aluminum concentration as a function of the aluminum cell base temperature for the VEECO Gen II MBE Chamber.

Table 6. Parameter Values for Eq. 56

Parameter	Value
B_0	1177.631
B_1	-30.461
t_1	2.723E-09

3.6.3 Growth Parameters for GaN/AlGaN HEMT Structures

The nitride growth parameters were optimized over the course of this project. Many of the growth parameters were adjusted and resulted in a large increase in structure quality. Again, the growth parameters of the samples grown are given in Appendix H.

Both unintentionally doped (UID) and semi-insulating (SI) substrates were used in this study. The substrates had different GaN templates that were grown on top of sapphire. The UID substrate had 3 - 5 μm thick GaN template grown by MOCVD while the SI substrate has a 3 – 5 μm thick GaN template grown by HVPE and doped with Fe. The Fe doping was used to compensate for the naturally occurring n-type condition of GaN grown on sapphire, thus reducing the number of free carriers in the AlGaN/GaN system. AFM was performed on the UID and SI substrates and the images are shown in Fig. 36 (a) and Fig. 36 (b) respectively. The SI substrate was found to be locally very flat where the UID substrate contained pits that measured ~5 nm in depth (see Fig. 36 (c)) and Fig. 36 (d)). Due to the Fe doping and flatter surfaces, samples grown on SI substrates were more suitable for GaN HEMT growth. A quantitative discussion of measurement results is given in Section 3.8.

A total of 3 samples were grown on SI substrates. A cross sectional diagram of NH62 and NH63 is shown in Fig. 37 (a) while a cross sectional diagram of NH64 is shown in Fig. 37 (b).

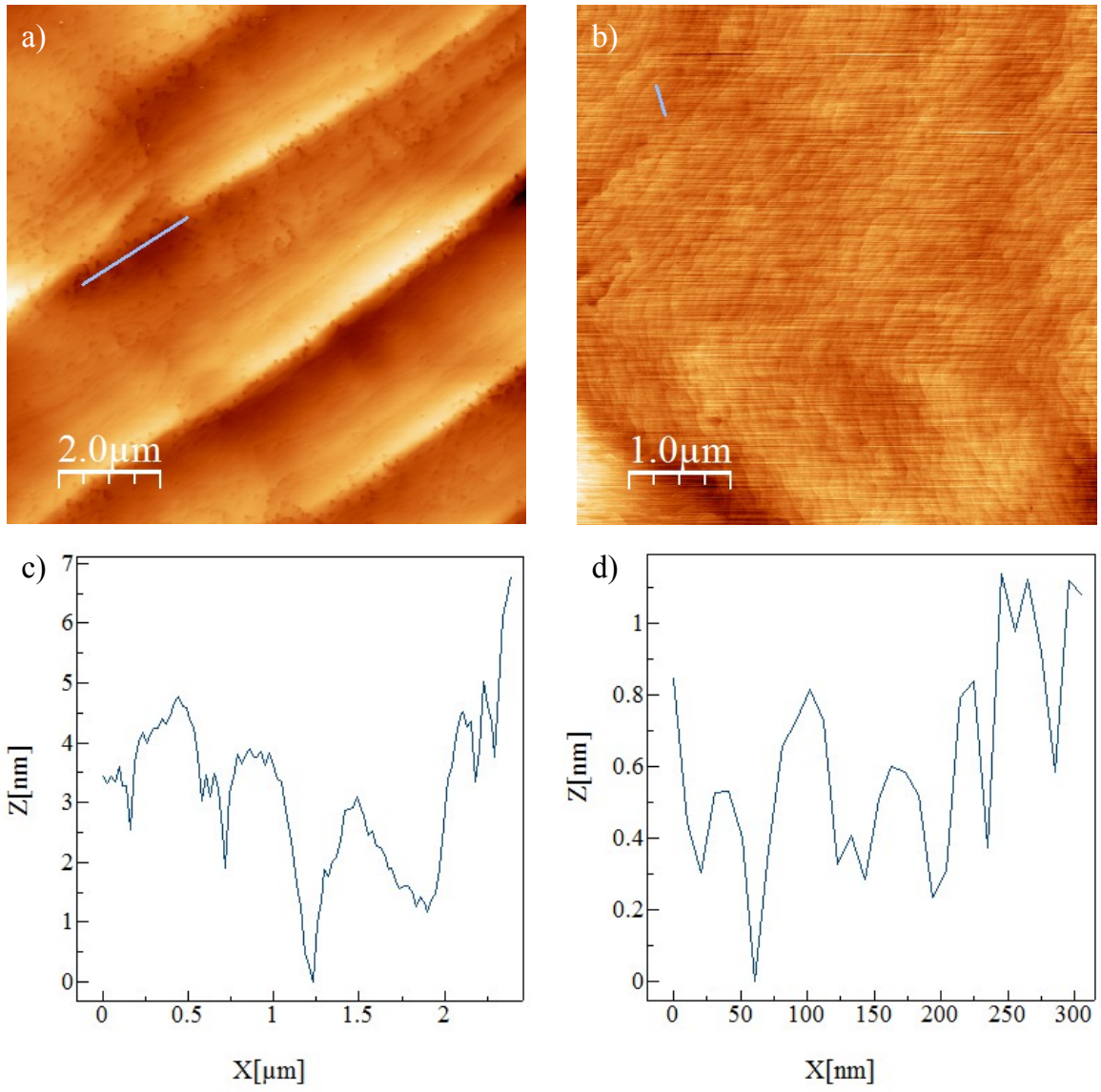

Fig. 36. AFM images of (a) UID and (b) SI GaN templates. (c) depth profile for the UID GaN template. (d) depth profile for the SI GaN template.

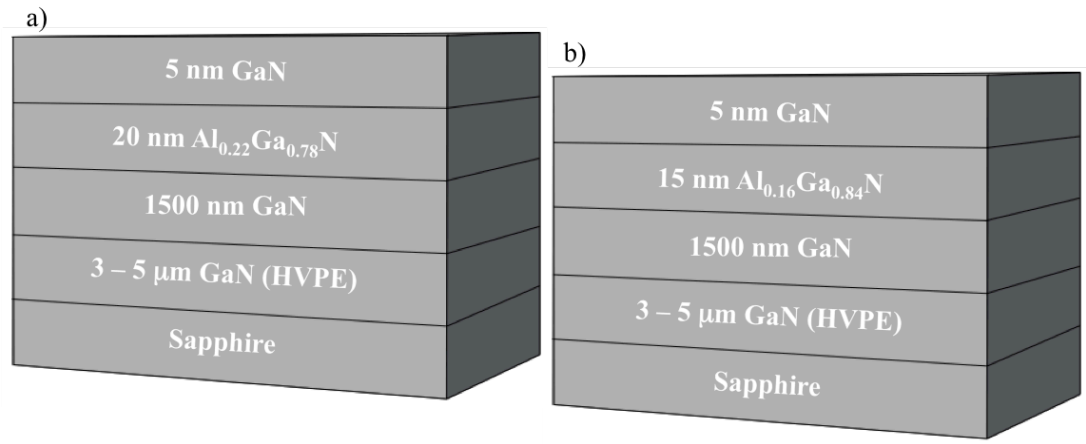

Fig. 37. Cross sectional diagrams of (a) NH62, NH63 and (b) NH64.

Substrate temperatures (T_{Sub}) only varied from 690 °C to 710 °C over the course of all growths in order to reduce calibration time. GaN growth can be carried out in the temperature range of 500 °C – 800 °C [23]. Research has shown that higher substrate temperatures may promote higher quality growth [35]. This is still debated, but growth at ~ 700 °C yielded high quality structures (μ_{Hall} ~ 1400 cm^2/Vs at room temperature).

The substrate temperature was the same (~ 700 °C) for the growth of both GaN and AlGaN in order to reduce annealing effects that can occur during temperature ramping needed at layer junctions. Of most concern was the interface roughness at the AlGaN-GaN junction.

In order to insure repeatable material growth, GaN stoichiometric tests were performed prior to each growth. A stoichiometric test allows for a repeatable substrate temperature, which can vary between growths due to the substrate mounting mechanism. The process for estimating the Ga flux required for stoichiometric GaN growth and obtaining the required N/Ga flux for high quality growth is explained below.

Recording RHEED intensity as a function of time was the method by which the Ga flux needed for stoichiometric GaN growth was estimated. When growing in the Ga rich regime,

excess Ga will accumulate on the sample surface, thus causing RHEED intensity to decrease due to shadowing alone, which is different from the growth oscillations depicted in Fig. 32. When growth is terminated, the excess Ga will begin to desorb. As Ga desorption occurs, the RHEED intensity will rise as the periodically aligned GaN crystal surface becomes more exposed.

RHEED intensity as a function of time for a Ga-N stoichiometric test is shown in Fig. 38. The shutter was initially closed for the first 80 seconds. The Ga and N shutters were then opened for a duration of 30 seconds. During growth, the RHEED intensity decreased. After 30 seconds, the shutters were then closed and the RHEED intensity began to increase. The initial recovery period was the time the RHEED intensity took to begin to increase rapidly. The total recovery period was the time it took for the RHEED intensity to recover to the initial intensity. The Ga flux that allowed for an initial RHEED recovery time of 0 seconds corresponded to the stoichiometric Ga flux.

A high Ga flux should be used for the initial data point taken for a stoichiometric test in order to prevent surface roughing that occurs when growing in the N rich regime. Stoichiometric tests should be repeated while decreasing the Ga flux until a Ga flux corresponding to a 0 second initial recovery time can be predicted. This process is depicted in Fig. 39. Three data points were collected for the Ga cell temperature (Ga flux and cell temperature are related by Eq. 55) as a function of the initial RHEED recovery time. A linear fit was performed. With a substrate temperature of 697 °C, a Ga cell temperature of 928 °C was required in order to achieve stoichiometric growth of GaN. In order to insure repeatable material growths, the same Ga cell temperature that achieved stoichiometric growth is required. This assured the desorption rate of Ga and thus the substrate temperature was equal between growths. A Ga cell temperature of 929 °C was used for this pre-growth calibration. In the above example concerning NH64, T_{Sub}

was increased so that a higher Ga flux was needed in order to account for the increased desorption.

The initial growths on UID substrates were carried out with Ga/N ratios around 6%. This was found to prevent large pits from penetrating the MBE layers and reaching the surface. As the buffer thickness increased, the amount of excess Ga required for a flat surface decreased. A Ga flux of 2.0% over the stoichiometric flux was found to yield high quality structures. The corresponding Ga cell base temperature at a substrate temperature of ~ 700 °C for 2.0% excess Ga is ~ 930 °C. Excess Ga accumulated on the surface at this flux but was removed with HCL as discussed in the following section.

The RF plasma power and nitrogen flow rate were the same for each growth. The plasma power was kept at 350 W with a nitrogen flow rate of 0.50 sccm. These settings allowed for a growth rate of 4 nm/min.

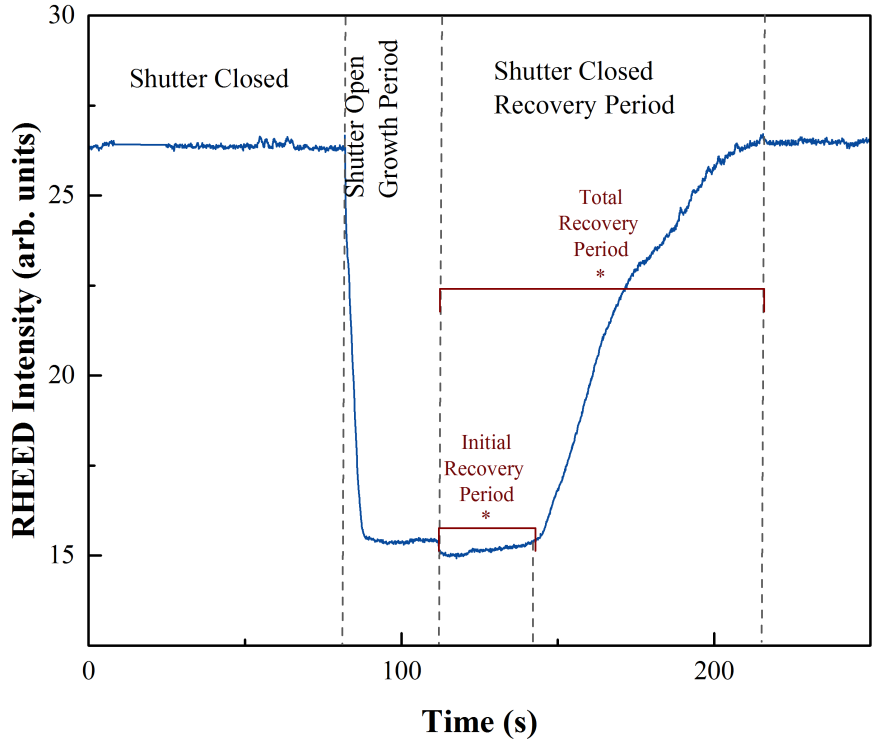

Fig. 38. RHEED intensity as a function of time.

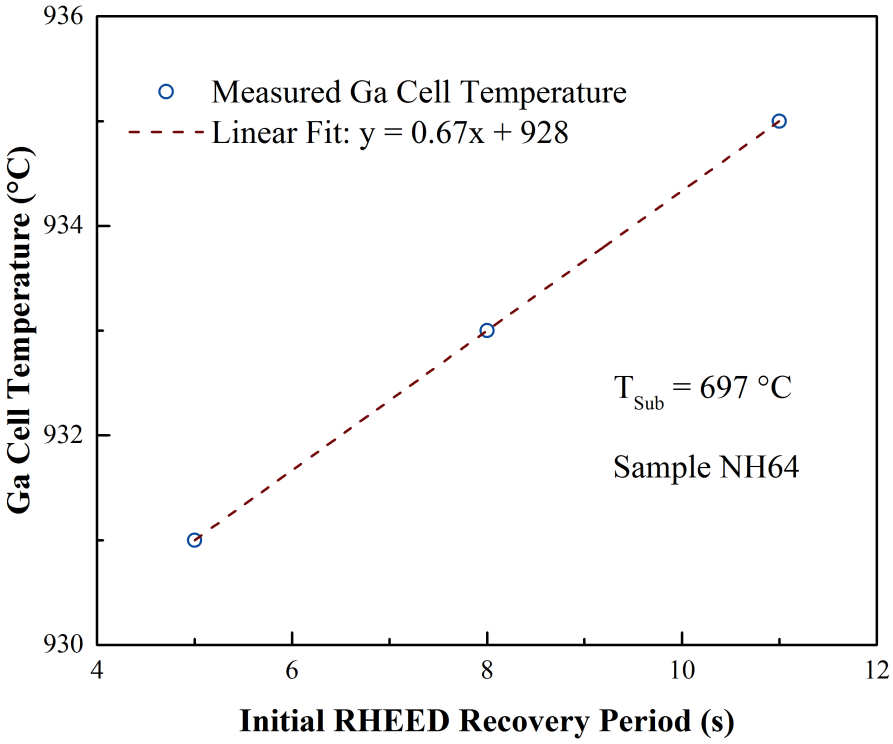

Fig. 39. Stoichiometric test for sample NH64.

3.7 Processing GaN-based Micro Hall Devices

Processing is a very important part of the device fabrication process. Poor processing techniques can lead to decreased device performance. In this section, sample cleaning, cutting, etching and metallization are described.

3.7.1 GaN Sample Cleaning

In order to grow structures with relatively flat surfaces, growth was carried out in the Ga rich regime [35]. As discussed in section 3.6, Ga droplets remained on the surface post growth and the droplets were removed prior to metallization. Hydrochloric acid (HCl) was suitable to use because it did not roughen the GaN surface while it etched excess Ga. A 25-minute HCl bath at room temperature has been found to remove Ga droplets from the GaN surface. Once removed from HCL, the samples were immediately placed in acetone. An ultrasonic cleaner was used to further remove loose debris from the sample. The sample was then rinsed in methanol and dried with N_2. AFM images before an HCL bath and after are shown in Fig. 40. The small dots in Fig. 40 (a) were Ga droplets, which had been removed in Fig. 40 (b).

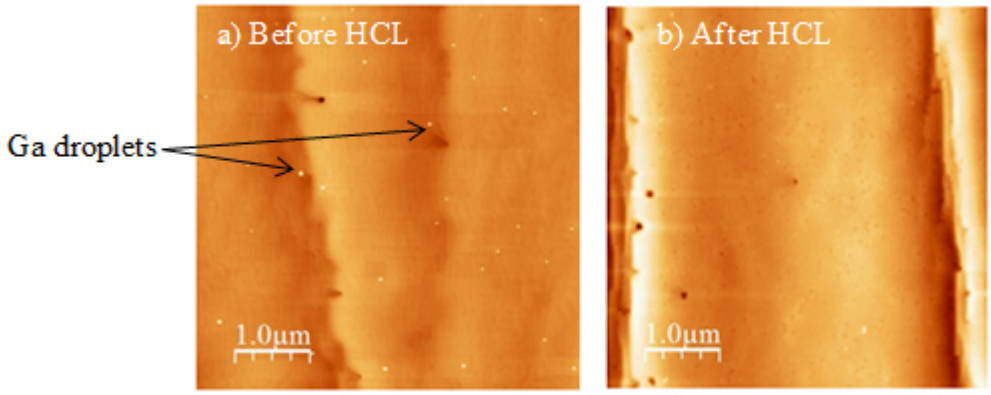

Fig. 40. AFM images before (a) and after (b) HCL etch.

3.7.2 GaN Sample Cutting

Once the excess Ga was removed from the surface, the sample was cut. The main consideration when cutting was the different sample sizes needed for proper characterization. The cuts are shown in Fig. 41. The first cut was to remove the area that was not exposed to growth due to overlap from the Molly block, which was 2 mm removed from the flat edges. There were three areas to consider when cutting:

1. 6 mm × 6 mm area for Hall measurements on the Lakeshore system.
2. 10 mm × 10 mm area to be patterned with Greek cross and TLM structures,
3. 6 mm × 10 mm area for C-V measurements.

Two methods of cutting are shown in Fig. 41. Fig. 41 (a) shows a cutting method that allows for the top half of the 10 mm × mm and a 6 mm × 6 mm piece to be cut from the center. Fig. 41 (b) shows a method for obtaining two 10 mm × 10 mm pieces. Since the Molly block held the sample at the edges, the most consistent growth was expected be at the center. All samples were cut with a Shirline saw (Model 5410).

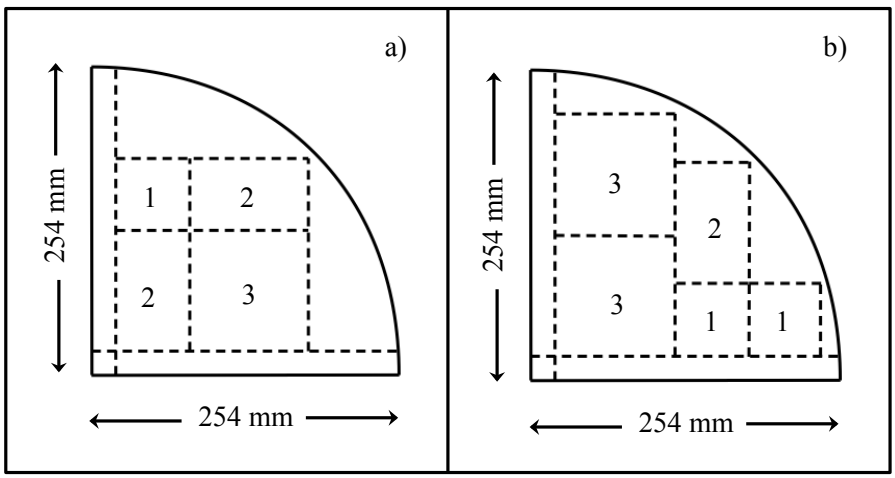

Fig. 41. Two methods for cutting 1/4 of a 2 inch wafer. Section 1 is 6 mm × 6 mm. Section 2 is 6 mm × 10 mm. Section 3 is 10 mm × 10 mm. (a) Allows for the 6 mm × 6 mm and half of the 10 mm × 10 mm to be in the middle. (b) Allows for two 10 mm × 10 mm pieces.

3.7.3 Processing GaN HEMT structures for Measurements made by Lakeshore Hall Measurement System

Hall measurements using the Lake Shore system were the first measurements to be made because of low processing requirements and the results indicated whether further characterization was needed. In order to conduct Hall measurements on the Lake Shore system, only contacts and wires need to be applied to the 6 mm × 6 mm samples. Indium, which can be applied quickly, was used for ohmic contacts. The In contacts were as small as possible and placed at the corners of the sample (see section 1.5.1). The contacts were annealed at 450 °C for 5 minutes. After annealing, gold wires were attached to the contacts by CircuitWorks two part conducting paste manufactured by Chemtronics. The paste was heated at 90 °C for 10 minutes. Fig. 42 is a picture of a 6 mm × 6 mm sample processed for Hall measurements on the Lake Shore measurement system.

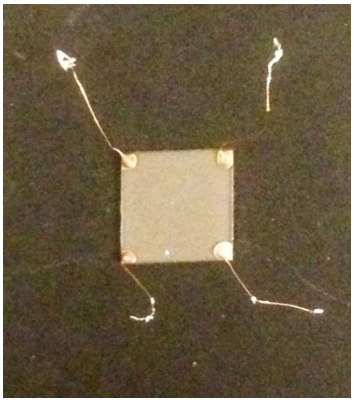

Fig. 42. Process 6mm^2 GaN HEMT structure for Hall measurements on a Lakeshore system.

3.7.4 Processing of GaN-based Micro-Hall Devices with Greek Cross Geometry and TLM Structures for Contact Optimization.

Processing of micro-Hall devices with Greek cross and TLM structures was a complex procedure that required optical photolithography and reactive ion etching (RIE). The preferred etching method was Cl based reactive ion etching (RIE) which can had an etch rate as high as 800 nm per minute [36]. SF_6 has also been shown to etch GaN by RIE, however; the rate is much slower than that of Cl (~10 nm/min.) due to nonvolatile GaF_X that forms during the etching process [37]. The calibration of the sputtering component of RIE was very important when considering the removal of GaF_x. RIE by SF_6 was the only etching method available for nitride structures available at the University of Arkansas. Samples were prepared for RIE by Cl in order to be etched at Texas Tech University. Processing steps were the same for both cases and are explained below.

Contacts are first applied to the 10 mm × 10 mm sample. In order to apply contacts, the sample was first patterned with photoresist (PR). AZ 5214 PR was used for processing because both positive and negative resists were needed. For metallization, the PR should be positive. The PR was spun on at 3000 rpm and then baked on a hotplate for 60 sec at 95 °C. The samples were then exposed to UV light for 18 seconds and developed by being placed in AZ 300 MIF developer for 60 seconds. After developing, the samples were cleaned with DI water and dried with N_2.

Metal was deposited in an Edwards Auto 306 electron beam (e-beam) evaporator. A cross-sectional diagram of the contacts is shown in Fig. 43. Lift-off was then performed by soaking the samples in acetone overnight. The unwanted metal was then removed by either agitation from a pipette or by placing the sample in a beaker containing acetone and then placing the

beaker in the ultrasonic cleaner for 1 to 3 seconds. The contacts were then annealed in an AG and Associates rapid thermal processor (rapid thermal anneal or RTA) for 30 seconds at 850 °C.

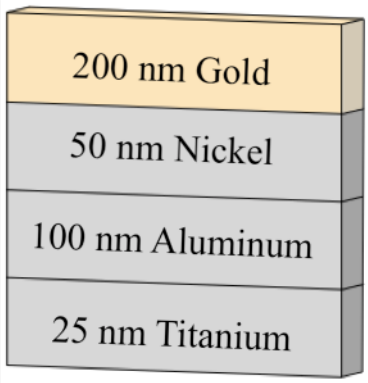

Fig. 43. Cross-sectional diagram of the ohmic contact structure for GaN capped devices.

Ti and Al created a good ohmic contact because of their similar work functions as listed in Table 7. Ti was used, even though the work function is greater than that of Al, because it reacts with N to form TiN. The N vacancies then created excess electrons. Therefore, the metal-semiconductor junction was highly doped. The excess electrons were then free to tunnel through the barrier, which decreased the contact resistance. The aluminum atoms diffused, thus the Al work function needed to be close to GaN as well. The nickel was an adhesion layer as well as a diffusion barrier because gold diffuses very rapidly [38]. The gold was deposited for reliable wire bonding.

Table 7. Work Functions for Metals Used for Schottky Contacts [39]

Material	Work Function (V)
Au	4.8
Al	4.28
Ni	5.15
Ti	4.33
GaN	4.1

500 nm of SiO_2 was then deposited on the 10 mm × 10 mm sample by method of plasma enhanced chemical vapor deposition. Then positive PR was applied by the method described above. The mask used for UV light exposure covered both contact and desired mesa areas. SiO_2 was etched by 5:1 buffered oxide etch (BOE) for 60 seconds. The remaining PR was removed by acetone.

A Ni mask, which was removed by $NH0_3$, was used as a final projective layer. In order to deposit a Ni mask on the mesa area, a negative PR was required. Again, AZ 5214 PR was used. The PR is spun on at 4000 rpm for 30 seconds. A prebake was performed on a hotplate at 100 °C for 60 seconds. Then UV exposure with the mask was performed for 6 seconds after which the sample was baked for 60 seconds at 110 °C. A flood exposure of 12 seconds was then required to make the PR negative. The sample was then developed by AZ 300 MIF developer for 90 seconds, rinsed in DI water and dried by N_2. A portion of a sample processed for Greek cross and TLM structures is shown in Fig. 44.

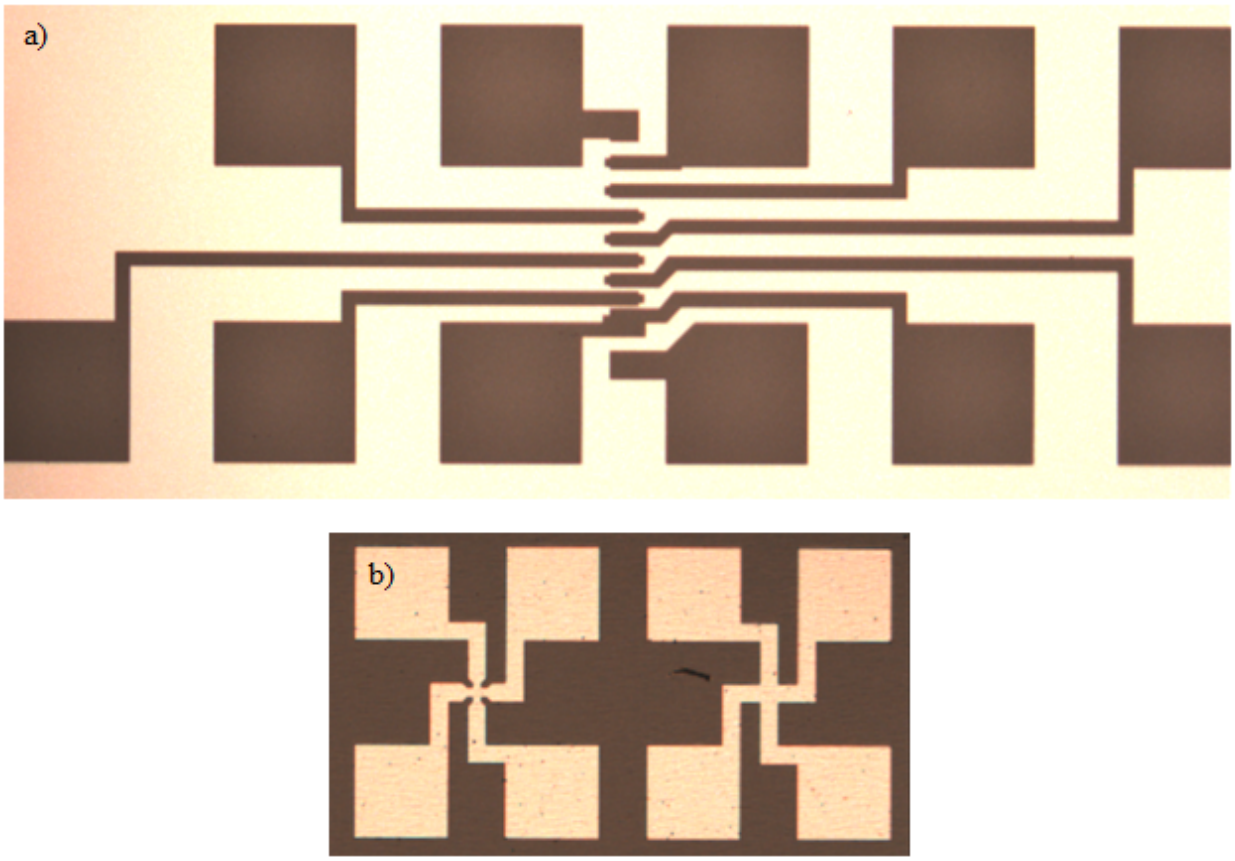

Fig. 44. (a) TLM structure. (b) Greek cross structures.

3.7.5 Processing Diode Structures for Capacitance – Voltage Measurements

Both ohmic and Schottky contacts were needed for C-V measurements. A negative voltage is applied to the Schottky contact and creates a depletion region. Charge at the metal-semiconductor junction and depletion region edge form a capacitance. An AC voltage is then superimposed onto the DC voltage causing changes the accumulated charge, Q. This change in charge with voltage is measured as a capacitance,

$$C = \frac{dQ}{dV} \tag{57}$$

An HP 4280 A 1MHz C meter/C-V plotter was used for C-V measurements.

The carrier concentration can then be extracted from C-V data by using [28]

$$N_{C-V} = \frac{C^3}{q\epsilon_0\epsilon}\frac{dV}{dC} \tag{58}$$

and the depth by

$$d = \frac{\epsilon_0\epsilon}{C} \tag{59}$$

where C is the measured capacitance per unit area, V is the applied voltage, and ϵ is the dielectric constant of the material. A picture of a processed sample for C-V measurements is shown in Fig. 45.

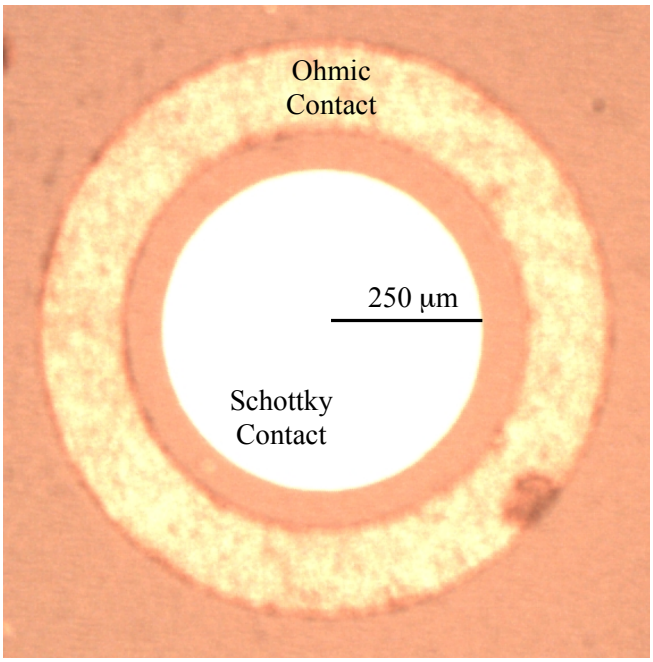

Fig. 45. Sample processed for C-V measurements.

In order to create a good Schottky contact, a large difference in work functions must be achieved. Due to the work function differences shown in Table 7, Ni metal was chosen as the Schottky contact. 200 nm of Au was deposited on top of the Ni for wire bonding. A cross section of the Schottky contact is shown in Fig. 46. I-V measurements were performed to test the quality of the Schottky contact. The IV data are shown in Fig. 47. The leakage current remained under 1 mA for reverse biasing up to 3 V. In reverse bias, the current remained low

due to the increased barrier for electrons in the semiconductor material. The barrier for electrons in GaN was lowered in the forward biasing condition. As the barrier lowered, the number of electrons with enough energy to overcome the barrier at the metal-semiconductor junction increased exponentially as shown in Fig. 47 [5]. An HP 4140 B pA meter/DC voltage source was used for obtaining I-V data.

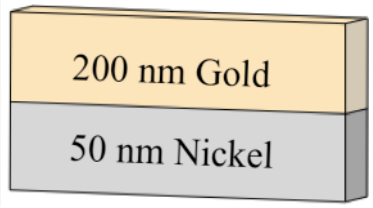

Fig. 46. Schottky contact cross section.

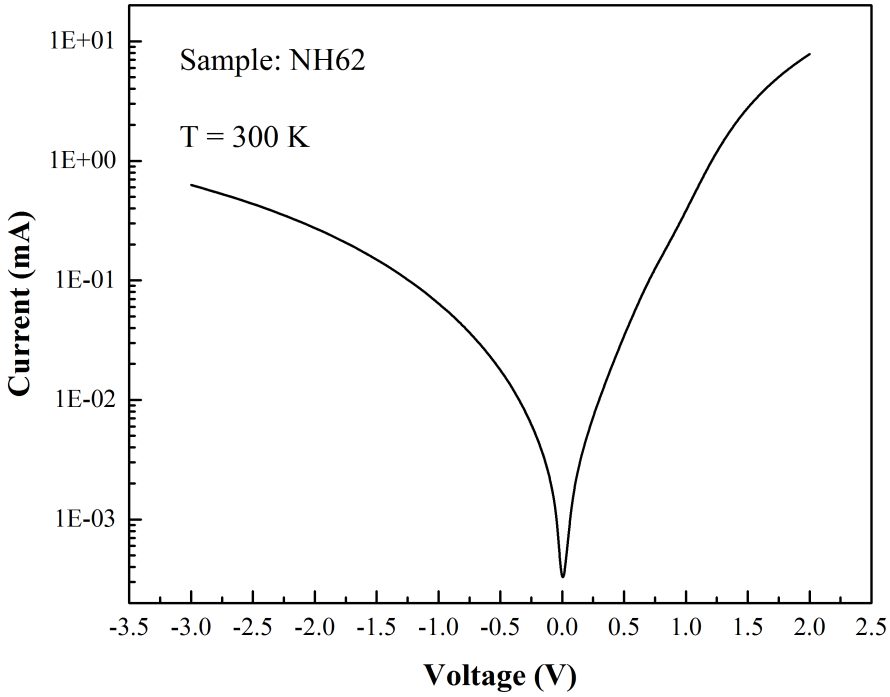

Fig. 47. I-V measurement results for GaN-based Schottky diode.

3.8 GaN-Based Micro-Hall Device Characterization Results

In the following sections, the detailed characterization of the GaN/AlGaN material system planned for fabrication of the micro-Hall device will be presented. The characterization techniques used for this research included atomic force microscopy (AFM), high resolution x-ray diffraction (HRXRD), Hall effect measurements, and C-V measurements. Data analysis from these measurement results is discussed below.

3.8.1 Surface Morphology Analysis for GaN Based HEMT Structures.

The surface morphology of each sample was analyzed by AFM and then compared to the substrate. Steps ranging in height from 10 nm – 25 nm were visible on the UID substrate surface as shown in Fig. 48 (a). Steps of a height of ~ 10 nm were also found on samples NH36 and NH50, both of which were grown on UID substrates. NH36 contains a 300 nm GaN buffer while NH50 contains a 1500 nm GaN buffer. Thus, buffer thickness did not improve the step height. Such steps did not appear on the SI substrates used in this research as shown in Fig. 36. From this analysis, a high quality substrate is critical for achieving a high quality (as flat as possible) surface.

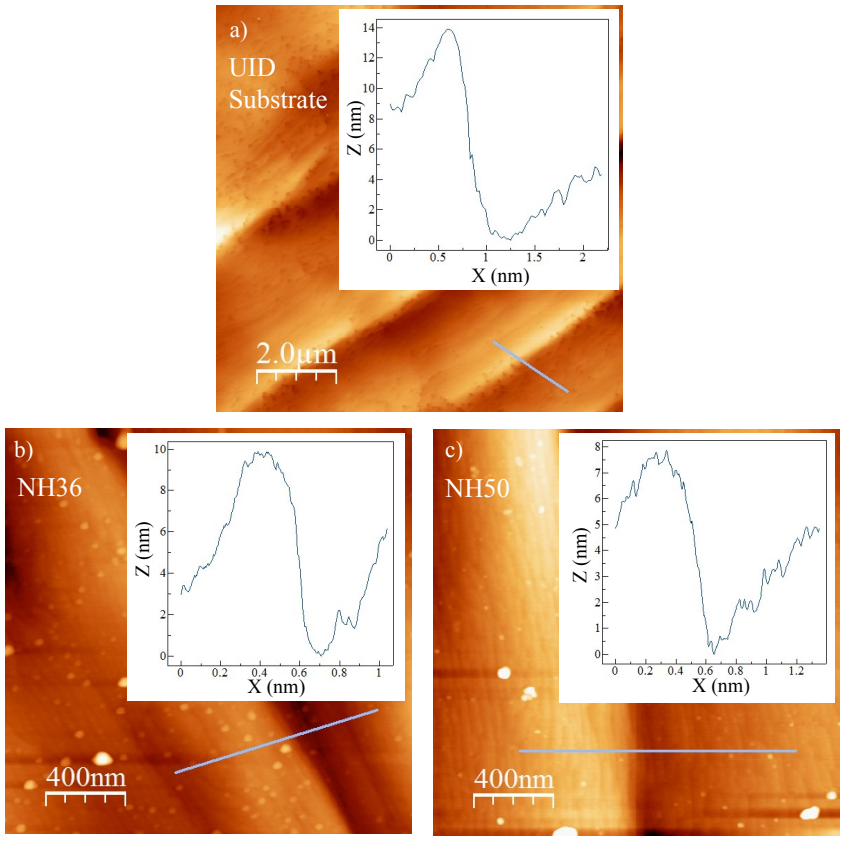

Fig. 48. AFM images of (a) UID substrate, (b) Sample NH36, and (c) sample NH 50.

AFM images and depth profiles of samples grown on UID substrates (NH36, NH39, and NH50) as well as samples grown on SI substrates (NH62, NH63, and NH64) are shown in Fig. 49. A large amount of excess Ga was found on the surface of NH36 due to a high Ga flux throughout the growth and inadequate HCl etching time. The HCl etching time was increased resulting decreased excess Ga found on the remaining sample surfaces.

A large number of pits at least 2 nm deep was found on the surface of NH39 and were likely due to threading dislocations that originated at the sapphire/GaN interface. These pits were likely deeper than 2 nm, as they appeared too narrow to be probed effectively by AFM. The difference in surface quality between sample NH36 and NH39 was most likely due a difference in substrate temperature caused by growths on different substrate holders. It was probable that

NH39 was grown at a higher substrate temperature and thus closer to the nitrogen rich regime. After the growth of NH39, stoichiometric calibrations were performed in order to achieve repeatable material growths. High quality surfaces were achieved after the growth of NH39 as shown in Fig. 49. Atomic terraces of a depth ~ 0.4 nm are found on the surface of NH50 – NH64, which is in agreement with lattice parameters for GaN.

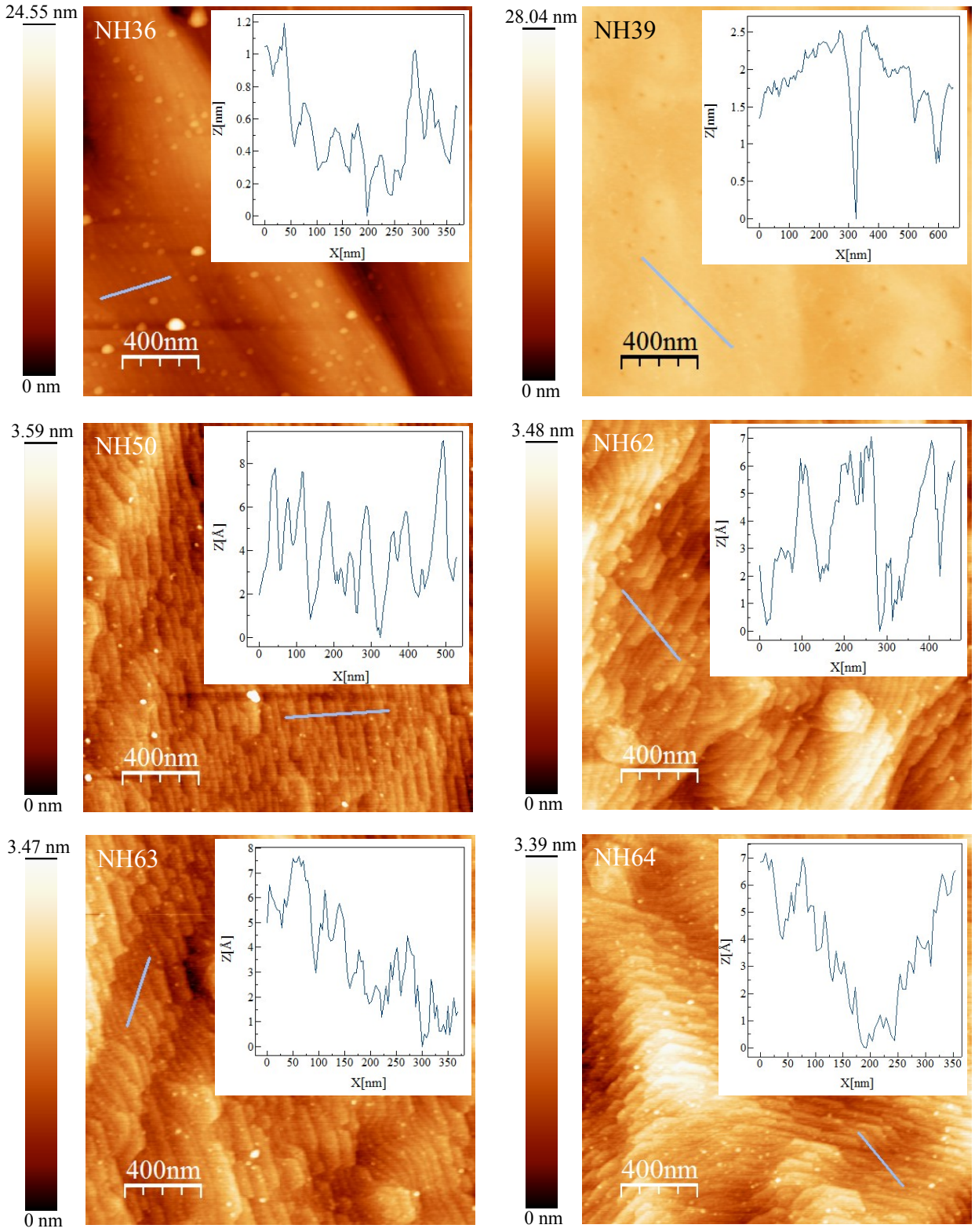

Fig. 49. AFM images for Samples NH36, NH39, NH50, NH62, NH63, NH64.

3.8.2Analysis of Strain and Aluminum Molar Fraction in the AlGaN Barrier of GaN HEMT Structures

In order to prevent additional defects from appearing within the sample, the AlGaN barrier should remain strained. Knowing the Al concentration within the barrier is also critical for understanding device performance. In order to determine the strain and Al concentration found in the AlGaN barrier, XRD was performed. From the XRD data, reciprocal space maps (RSM) were extracted. The intensity plotted in the RSM varried in the x direction for varying strain intensities and in the y direction for varying Al molar fractions due to the different lattice parameters for GaN and AlN. From the RSM shown below, the peaks in intensity that corresponded to a fully strained AlGaN barrier and the Al molar fraction for NH62 and NH64 are ~21% and ~13% respectively. Due to the low Al concentration in sample NH63, it was difficult to accurately predict the Al concentration in the AlGaN layer.

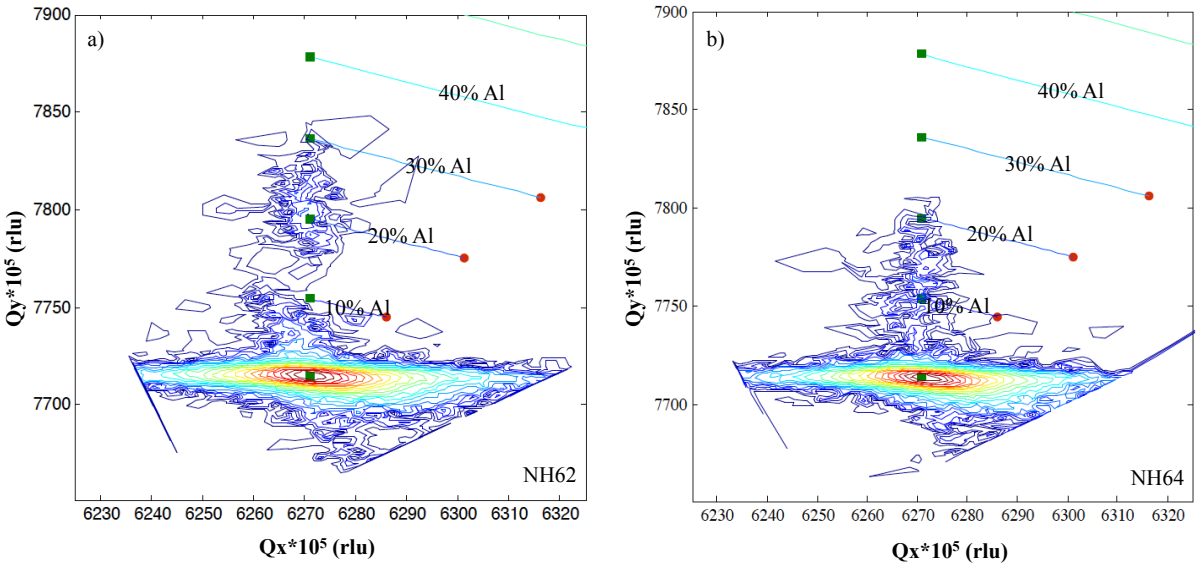

Fig. 50. Reciprocal Space map for (a) NH62 and (b) NH64

3.8.3 Hall and C-V Measurement Results for GaN HEMT Structures

Table 8 shows Hall measurement results for six samples grown during this project. The lower sheet electron density of NH36 when compared to NH39 is was thought to be due to a thin AlN layer atop the GaN template. A larger reduction in sheet density from NH39 to NH50 was achieved by increasing the buffer thickness from 300 nm to 1500 nm. Finally, the electron sheet density was reduced by 96.64% from NH50 to NH62 by using a semi-insulating (SI) substrate (GaN doped with Fe on sapphire). Hall measurements taken during this project showed that GaN grown on an unintentionally doped (UID) substrate had a high carrier concentration while GaN grown on SI substrate was semi-insulating. This was in agreement with the explanation that donor-like surface states were the likely source of the 2DEG for high mobility samples grown on SI substrates.

The carrier concentration as a function of temperature was obtained by a Lakeshore Hall effect measurement system and is shown in Fig. 51 for samples grown on SI substrates. The data followed an exponential temperature dependence that was due to the lowering of the Fermi level when temperature decreased [5]. The minimum carrier concentration recorded during this project was 3.66 x 10^{12} cm^2/Vs at 8 K for sample NH62 consisting of a 15 nm $Al_{0.13}Ga_{0.87}N$ barrier.

The carrier profile extracted from C-V measurements by using Eq. 58 and Eq. 59 for sample NH62 is shown in Fig. 52. The peak carrier density (location of 2DEG) is located at a depth of 22 nm. This is in agreement with the estimated layer thicknesses of sample NH62.

Table 8. Hall Effect Measurement Results for Six Samples Grown During this Project

		Substrate					
		UID MOCVD GaN Template on Sapphire			SI HVPE GaN Template on Sapphire		
Property	Units	NH36*	NH39	NH50	NN62	NH63	NH64
Barrier Thickness	nm	20	20	20	20	20	15
Al Composition	%	22	22	22	22	22	13
Buffer Thickness	nm	300	300	1500	1500	1500	1500
n_{2D} at 290 K	cm^{-2}	4.11E+14	4.30E+14	3.30E+14	1.11E+13	1.02E+13	5.76E+12
n_{2D} at 8 K	cm^{-2}	3.26E+13	3.80E+13	1.50E+13	6.25E+12	6.48E+12	3.66E+12
μ_{Hall} at 290 K	cm^2/Vs	300	250	340	1220	1400	1330
μ_{Hall} at 8 K	cm^2/Vs	2770	2100	8300	14 600	15 300	19 450

* Contains a 5 nm AlN layer above GaN template

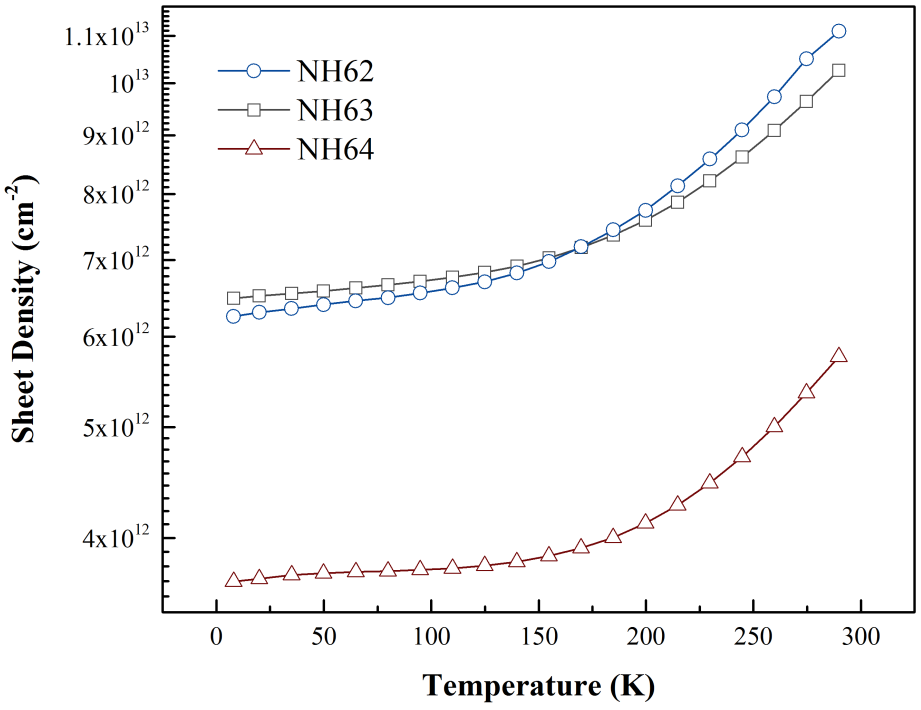

Fig. 51. Sheet density as function of temperature for samples grown on SI substrates.

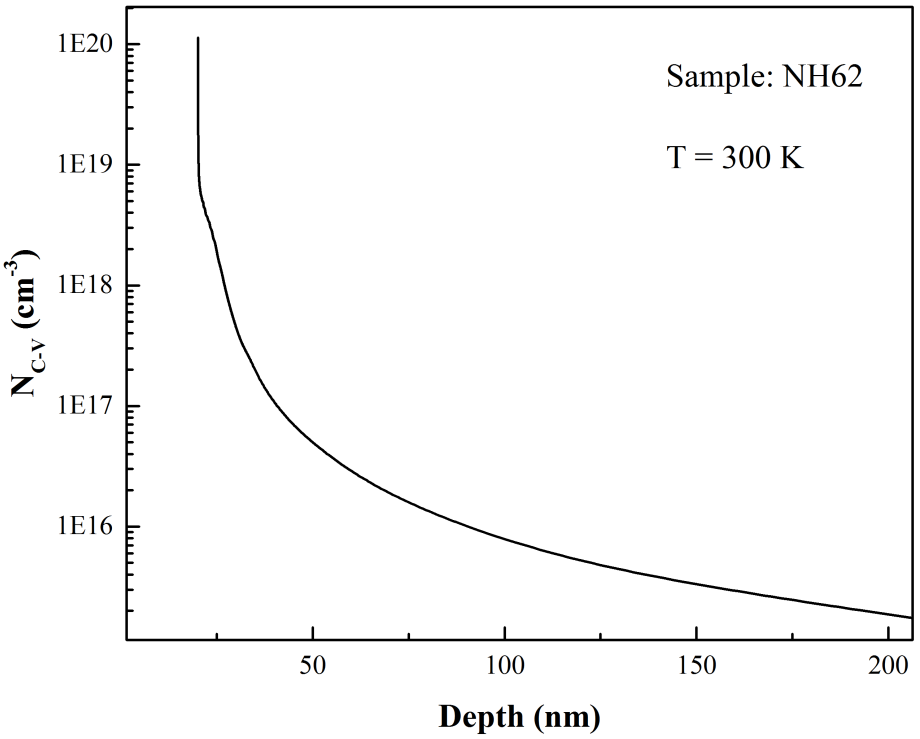

Fig. 52. Carrier profile obtained from CV measurement data.

For a structure containing a 2DEG, the mobility verses temperature curve will have the trend that is shown in Fig. 53. A reduction of phonon scattering was the cause of the rise in mobility as the temperature decreased from 300 K to 150 K. As the temperature decreased, the thermal velocity of the charge carriers also decreases. In a sample without confined electrons, the mobility would decreased for temperatures below 150 K because of the increased Coulomb scattering that occurs when the thermal velocity of the electrons decrease [5]. However, for a sample containing a 2DEG, the effect of Coulomb scattering is very small. Thus, the mobility of electrons does not decrease for temperatures below 150K [19].

The maximum room temperature mobility obtained during this project was 1400 cm^2/Vs. The highest room temperature mobilities are close to 2000 cm^2/Vs for GaN-based HEMT structures containing 20% Al within the AlGaN barrier and operating at room temperature [19].

Only the low temperature mobility increased from sample NH63 to NH64 even with a large reduction of sheet density. This was most likely due to a reduction in alloy scattering due to a reduction in the barrier thickness and Al concentration in the AlGaN barrier [19] [21]. One of the limiting factors for mobility at low temperature can be impurity scattering from defects within the device volume [22].

Improvements to the low temperature mobility may be achieved by using substrates with thicker GaN templates. Increasing the template thickness will reduce the number of threading dislocations within the sample. Threading dislocation can act as charge centers that penetrate through the device volume. Thus, threading dislocation can act as scattering centers within the QW. The threading dislocation density for a 40 μm thick GaN template grown on sapphire by method of HVPE is ~10^8 cm^{-2} [22]. The GaN templates used for growth during this project were 5 μm so the threading dislocation density should be higher [21]. The maximum mobility obtained during this project was 19,450 cm^2/Vs at 8 K by the use of a GaN/$Al_{0.13}Ga_{0.77}N$/GaN HEMT structure, which is within 0.09% of the state of the art found in recently published papers [40]. Further enhancements to low temperature mobility could be made by decreasing the Al molar fraction in the AlGaN barrier to the range of 5% – 10%.

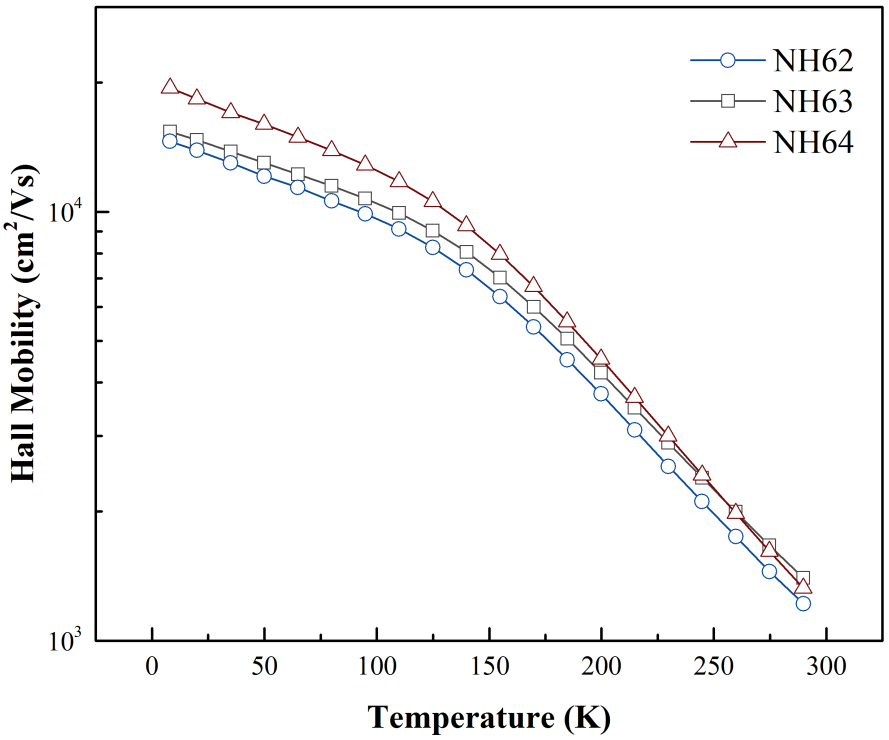

Fig. 53. Hall mobility as a function of temperature for samples grown on SI substrates.

To summarize this part of my research, it was demonstrated that a GaN/AlGaN material system could be promising for fabrication of micro-Hall devices. A two-dimensional electron gas was realized at the GaN/AlGaN interface without the use of dopants. The highest room temperature mobility of 1400 cm^2/Vs was achieved with a GaN/$Al_{0.21}Ga_{0.79}N$/GaN HEMT structure. The sheet density measured for this structure was 1.02 x 10^{13} cm^{-2}. Such high quality heterstructures were obtained by careful optimization of the growth conditions, including Ga/N flux ratio, growth temperature, and growth rates (see Apendix H). A Ga/N flux ratio of 2.0% above stoichiometry, a growth temperature of 690 °C, and a growth rate of 4 nm/min was found to be optimal for obtaining the desired electrical characteristics as well as quality surface morphology. These studies indicate that the thickness of the GaN buffer layer is critical for achieving low densities of 2DEG, which are critical for obtaining high magnetic sensitivities of

the magnetic sensor. The thickness of the GaN buffer affected the dislocation densities located at the depth of the QW and thus, device characteristics. Along with GaN buffer thickness, the composition of Al found in the AlGaN barrier along with the barrier thickness were critical for gaining high electron mobilities. Analysis by AFM, supported by detailed studies of reciprocal space maps of the grown materials, confirmed high quality (based on mobility) growth of the strained AlGaN layer on top of the GaN buffer. These studies were in agreement with the temperature dependent Hall effect measurements.

Chapter 4: Conclusions and Future Work

GaAs and InGaAs QW micro-Hall devices were fabricated and detailed analysis of device characteristics were performed over a wide temperature and frequency range. Temperature dependent low frequency noise measurements were made and two active traps with activation energies of 0.40 eV and 0.57 eV were discovered for the InGaAs QW device. It was determined that the active traps were the cause of magnetic field detection degradation due to increases in noise from the generation-recombination process. The detection limit of the magnetic field was estimated to be as low as 6.2×10^{-8} T at room temperature.

High absolute sensitivities for devices with an active area of 40 μm^2 where found to be 0.70 V/T and 0.32 V/T for the temperatures of 80 K and 495 K. Magnetic sensitivities of 1362 V/T/A and 626 V/T/A where found at 80 K and 495 K, respectively. At temperatures above 500 K, the absolute sensitivity decreased by 59% from 500 K to 550 K. The absolute sensitivity and magnetic sensitivity found at a temperature of 550 K were 0.14 V/T and 274 V/T/A. In order to achieve higher device performance at high temperatures, material systems containing a larger band gap were studied.

Development of GaN/AlGaN material systems as candidates for micro-Hall device fabrication was investigated. From analysis of temperature dependent Hall effect measurements, a two-dimensional electron gas forming at the GaN-AlGaN interface was demonstrated. In order to obtain high quality GaN/AlGaN HEMT structures, growth conditions including Ga/N flux ratios and growth temperatures were optimized. Using the growth conditions of a Ga/N flux ratio of 2.0%, a growth temperature of 690 °C, and a growth rate of 4 nm/min achieved mobilities as high as 1400 cm^2/Vs at room temperature. From these studies, the role of the GaN buffer thickness was determined to be critical for achieving the lowest electron sheet densities,

which are required for obtaining high magnetic sensitivities of the micro-Hall devices. Changing the Al concentration in the AlGaN layer as well as the AlGaN layer thickness was also determined to be a valid method to further alter the density of the 2DEG. AFM and XRD studies further indicate that high quality strained AlGaN was grown on GaN

Comparing the results from Chapter 2 and 3, the InGaAs QW device had an 82% higher mobility than the GaN-based structures. A mobility of 7,980 cm^2/Vs at 300 K was recorded for the InGaAs QW device while the highest recorded mobility at 300 K for the GaN-based device is 1,400 cm^2/Vs. At this point in the investigation into GaN based devices, it is reasonable to conclude the InGaAs QW device is superior to that of GaN in terms of its sensitivity and low frequency noise characteristics. However, the GaN/AlGaN system is more promising for operation in harsh environments such as high temperatures and high electric fields due to a larger band gap and comparably high electron drift velocities.

Further research into the processing of GaN HEMT structures is required in order for an accurate comparison of GaN-based and InGaAs QW micro-Hall devices. These processing techniques include dry etching by RIE, contact optimization, and SiO_2 deposition/etching.

RIE recipes using both Cl and F gases for GaN/AlGaN etching will be developed. Results from the electrical characterization performed on samples etched by Cl and F will be studied in order to determine the gas most suitable for etching GaN and AlGaN.

Additional research into surface preparation and metallization techniques is needed for GaN structures. Surface cleaning techniques will be explored in order to achieve the most suitable surface conditions for metallization. Multiple metal contact structures should be studied in order to determine the structure that allows for the lowest contact resistance. Not only should the contact structure be studied, but also the annealing times and temperatures for each contact.

Sample preparation and contact optimization will play an import role in assuring the highest quality micro-Hall devices can be achieved.

Once processing of GaN-HEMT structures has been optimized, full characterization of GaN-based micro-Hall devices as well as reliability studies and bandwidth testing for the InGaAs QW device should be performed. At this time a comparison of InGaAs QW and GaN-based micro-Hall devices cannot be made.

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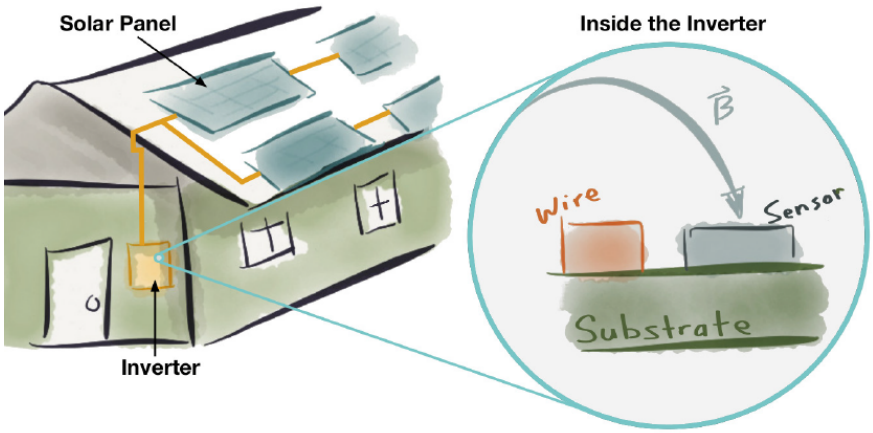
Appendix A: Description of Research for Popular Publication

Passive elements are an Aggressive Solution to Current Sensing

By Thomas White



The efficiency of electronic devices is very important, especially for applications such as inverters found in solar panels. Solar panels are a source of DC electricity that most often need to operate as an input to AC system, such as a home. Solar panels are less than 50% efficient to start with and therefore require as much help as they can get in order to be a valid source of DC electricity. Dr. Alan Mantooth and Mr. Thomas White at the University of Arkansas have been trying to help solar panel systems by improving the efficiency of the inverters required for changing DC to AC.

"At this time cost effective changes in the efficiency of solar cells are tough to come by. That's why we are looking into the inverters," says Mr. White.

The help is provided by improvements in current sensing technology. Current sensors are used for circuit protection that is needed in order to prevent expensive equipment from current overload. Current sensors can also allow for an increase in equipment lifetime.

But how can improving current sensor technology increase the efficiency of the inverter? By decreasing the heat created by the inverter. Typically, resistors are used to sense current in DC applications. When current passes though a resistor, the temperature of the resistor will rise. The heat is wasted power that could be used by the home.

Another large market that requires efficient inverters is the automotive industry, more specifically, the hybrid and electrical vehicle market. Often is the case that AC motors power hybrid and electric cars. The large batteries used to drive the motors are DC, thus require an inverter.

In the case of inverters found in solar panel systems or hybrid/electric vehicles, a robust current sensor that can operate at high temperatures is required. Researchers at the University of Arkansas use indium gallium arsenide (InGaAs) psuedomorphic high electron mobility transistor (pHEMT) structures to achieve these requirements.

The type of current sensor chosen to compete with resistors is a Hall effect sensor. Hall effect sensors work by sensing the magnetic field produced by a current carrying wire. The magnetic field of the wire is proportional to the current passing through it. The InGaAs pHEMTs

can sense current in the 10's of ampere range and only need 500 μA to do so. The efficiencies gained here may only be 2 – 3%, but in this industry that's aggressive.

Appendix B: Executive Summary of Newly Created Intellectual Property

The intellectual property created during this research is listed and discussed below.

1. The growth recipes used to grow GaN HEMT structures. The growth process for GaN HEMT structures containing a AlGaN layer with between 15% and 21% was optimized. The process discussed in this thesis resulted in state of the art mobilities (within 0.09%)
2. The processing recopies for GaN basebased HEMT structures. These recipes in lithography, etching, and metallization.

Appendix C: Potential Patent and Commercialization Aspects of listed Intellectual Property Items

There are no potential patents resulting from this work. GaN HEMT structures have been previously investigated by other groups. While GaN-based Hall effect sensors are not currently commercially available, GaN-based transistors with similar structures are.

Appendix D: Broader Impact of Research

D.1 Applicability of Research Methods to Other Problems

The research method presented in this thesis is applicable to research performed in the areas of material growth, device processing, and device characterization. The nitride growth calibrations performed during this research is valuable for those who pursue nitride growth. The processing techniques discussed in this thesis are mostly applicable to nitrides as well. However, some aspects such as SiO_2 deposition are valuable for many fields. The device characterization techniques presented in this thesis is applicable to most fields concerning electron transport properties of semiconductors.

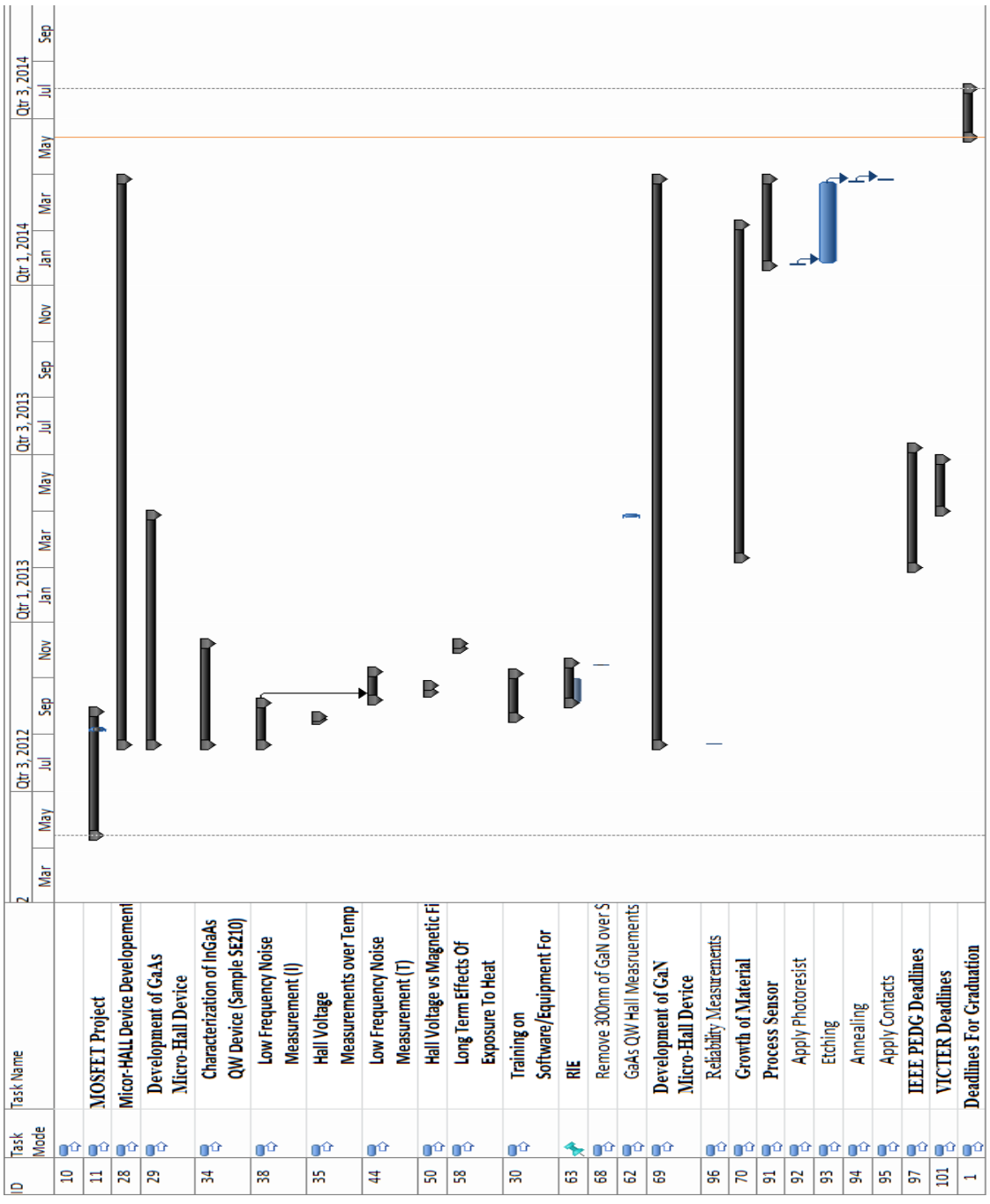
D.2 Impact of Research Results on U.S. and Global Society

This research could result in increasing the output of solar panel systems, thus reducing the amount of power generation needed. The Hall effect sensors presented in this thesis could also increase the efficiency of electric and hybrid vehicles.

D.3 Impact of Research on the Environment

This research does not have any adverse impact on the environment.

Appendix E: Microsoft Project for MS MicroEP Degree Plan



Appendix F: Identification of All Software Used in Research and Thesis Generation

Computer #1:
Model Number: MacBook Pro A1286
Serial Number: C02G57EVDRJD
Location: Home
Owner: Thomas White

Software #1:
Windows 7 Home Premium
Purchased: by Thomas White

Software #2:
Microsoft Office 2010
Purchased by: Thomas White

Software #3:
Microsoft Office 2011 Mac
Purchased by: Thomas White

Software #4:
OriginLab Origin Pro 9.0 Student Edition
Purchased by: Thomas White

Software #5:
VESTA
Free

Software #6:
Synopsys Saber RD
Purchased by: Free

Software #7:
iOS Productivity Suite
Purchased by: Thomas White

Software #8:
LT Spice IV
Free

Software #9
WSxM
Free

Computer #2:

Model Number: iPad A1395
Serial Number: DMQGLYS4DFHW
Location: Home
Owner: Thomas White

Software #1:

idraw for iPad
Purchased by: Thomas White

Software #2

Paper by FiftyThree
Purchased by: Thomas White

Appendix G: All Publications Published, Submitted and Planned

The following reference was submitted during this project.

T. White, V. Kunets, Y. Hirono, M. Ware, A. Mantooth, and G. Salamo, “High Performance Quantum Well Micro-Hall Device for Current Sensing in Inverters,” presented at the IEEE Symposium on Power Electronics for Distributed Generation (PEDG), 2013.

Appendix H: Growth and Processing Logs for Samples Listed in Table 8

In this Appendix, the growth logs for samples listed in Table 7 are given. The substrate temperatures (T_{Sub}) listed in each log are measured by the thermocouple providing information to the Eurotherm temperature controller. Temperature measurements made by the Pyrometer were found to be ~ 100 °C colder and are the temperatures measured by the thermocouple.

NH36

	Tsub (°C)	Ga 2 Base (°C)	Al Base (°C)
GaN Cap 5 nm	802	932	-
$Al_{0.22}Ga_{0.78}N$ Barrier 20 nm	802	932	1015
GaN Buffer 300 nm	802	931-934	-
AlN 5 nm	802	-	1049

Substrate: UID MOCVD GaN Template on Sapphire
Molly Block Number: 2
Plasma Power: 350 W
N_2 Flow Rate: 0.5 sccm
Growth Rate: 4 nm/min.
Growth Chamber Pressure: ~2.9E-6 Torr

Measured Sample Size: 6 mm^2

Contac Metal: Indium
Anneal Tempearture: 450 °C
Anneal Time: 5 min.

NH39

	Tsub (°C)	Ga 2 Base (°C)	Al Base (°C)
GaN Cap 5 nm	800	935	-
$Al_{0.22}Ga_{0.78}N$ Barrier 20 nm	800	935	1015
GaN Buffer 300 nm	800	932-935	-

Substrate: UID MOCVD GaN Template on Sapphire
Molly Block Number: 2
Plasma Power: 350 W
N_2 Flow Rate: 0.5 sccm
Growth Rate: 4 nm/min.
Growth Chamber Pressure: ~2.9E-6 - 3.2E-6 Torr

Measured Sample Size: 6 mm^2

Contac Metal: Indium
Anneal Tempearture: 450 °C
Anneal Time: 5 min.

NH50

	Tsub (°C)	Ga 2 Base (°C)	Al Base (°C)
GaN Cap 5 nm	800	929	-
$Al_{0.22}Ga_{0.78}N$ Barrier 20 nm	800	929	1015
GaN Buffer 1500 nm	800	929	-

Substrate: UID MOCVD GaN Template on Sapphire
Molly Block Number: 2
Plasma Power: 350 W
N_2 Flow Rate: 0.5 sccm
Growth Rate: 4 nm/min.
Growth Chamber Pressure: ~3.2-6 Torr

Measured Sample Size: 6 mm^2

Contac Metal: Indium
Anneal Tempearture: 450 °C
Anneal Time: 5 min.

NH62

	Tsub (°C)	Ga 2 Base (°C)	Al Base (°C)
GaN Cap 5 nm	794	929	-
$Al_{0.22}Ga_{0.78}N$ Barrier 20 nm	794	929	1015
GaN Buffer 1500 nm	794	934-932*	-

Substrate: SI HVPE GaN Template on Sapphire
Molly Block Number: 1
Plasma Power: 350 W
N_2 Flow Rate: 0.5 sccm
Growth Rate: 4 nm/min.
Growth Chamber Pressure: ~3.25E-6 Torr

Measured Sample Size: 6 mm^2

Contac Metal: Indium
Anneal Temperature: 450 °C
Anneal Time: 5 min.

* Linear ramp down of Ga 2 base for the first 140 nm. Ga 2 base remained at 932 °C for the remainder of buffer growth.

NH63

	Tsub (°C)	Ga 2 Base (°C)	Al Base (°C)
GaN Cap 5 nm	796	929	-
$Al_{0.21}Ga_{0.79}N$ Barrier 20 nm	796	929	1015
GaN Buffer 1500 nm	796	931-930*	-

Substrate: SI HVPE GaN Template on Sapphire
Molly Block Number: 1
Plasma Power: 350 W
N_2 Flow Rate: 0.5 sccm
Growth Rate: 4 nm/min.
Growth Chamber Pressure: ~2.93E-6 Torr

Measured Sample Size: 6 mm^2

Contac Metal: Indium
Anneal Tempearture: 450 °C
Anneal Time: 5 min.

* Ga2 base temperature was altered depending on RHEED image.

NH64

	Tsub (°C)	Ga 2 Base (°C)	Al Base (°C)
GaN Cap 5 nm	796	929	-
$Al_{0.13}Ga_{0.87}N$ Barrier 15 nm	796	929	1002
GaN Buffer 1500 nm	796	929	-

Substrate: SI HVPE GaN Template on Sapphire
Molly Block Number: 1
Plasma Power: 350 W
N_2 Flow Rate: 0.5 sccm
Growth Rate: 4 nm/min.
Growth Chamber Pressure: ~2.93E-6 Torr

Measured Sample Size: 5 mm^2

Contac Metal: Indium
Anneal Tempearture: 450 °C
Anneal Time: 5 min.